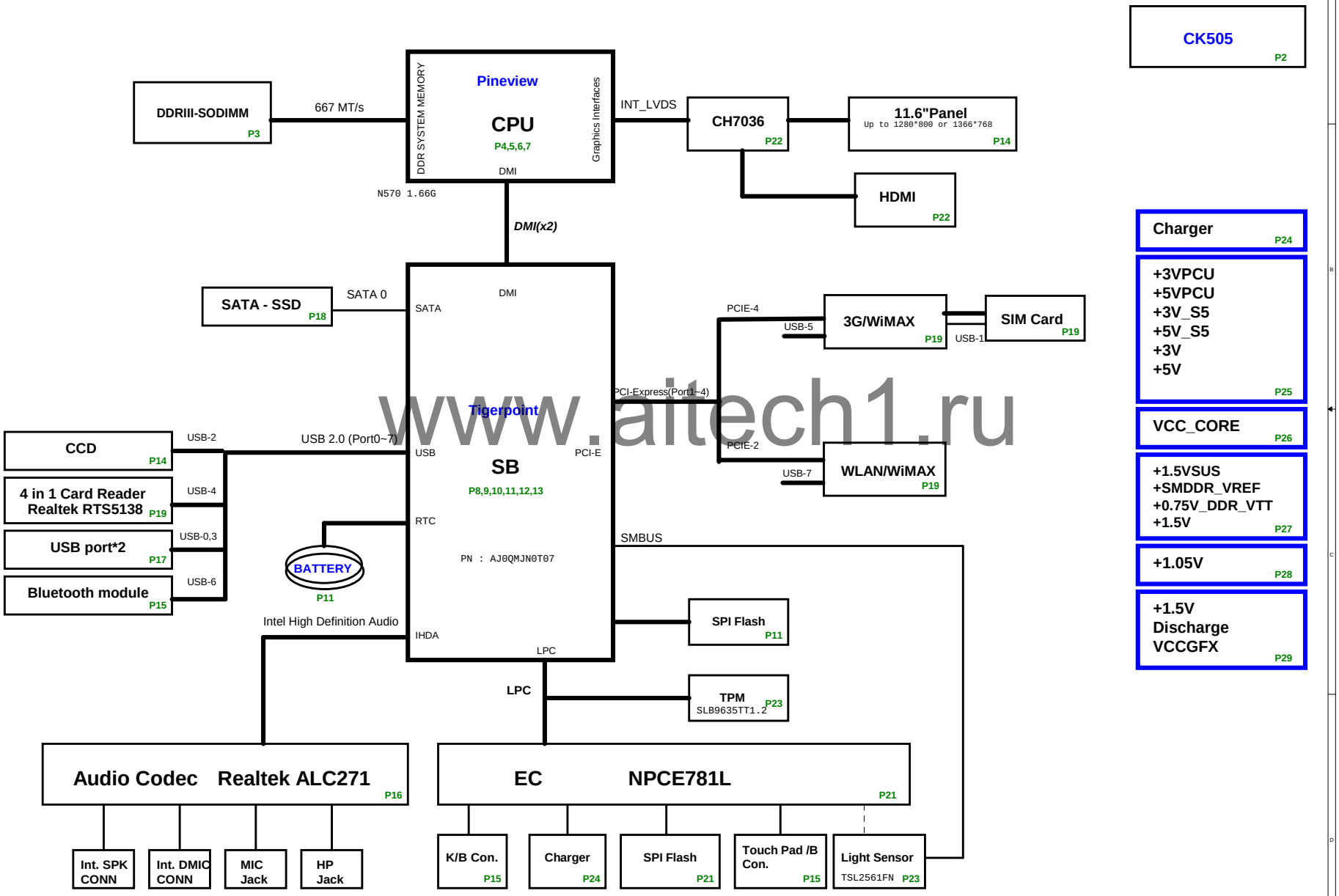
ZGB Block Diagram



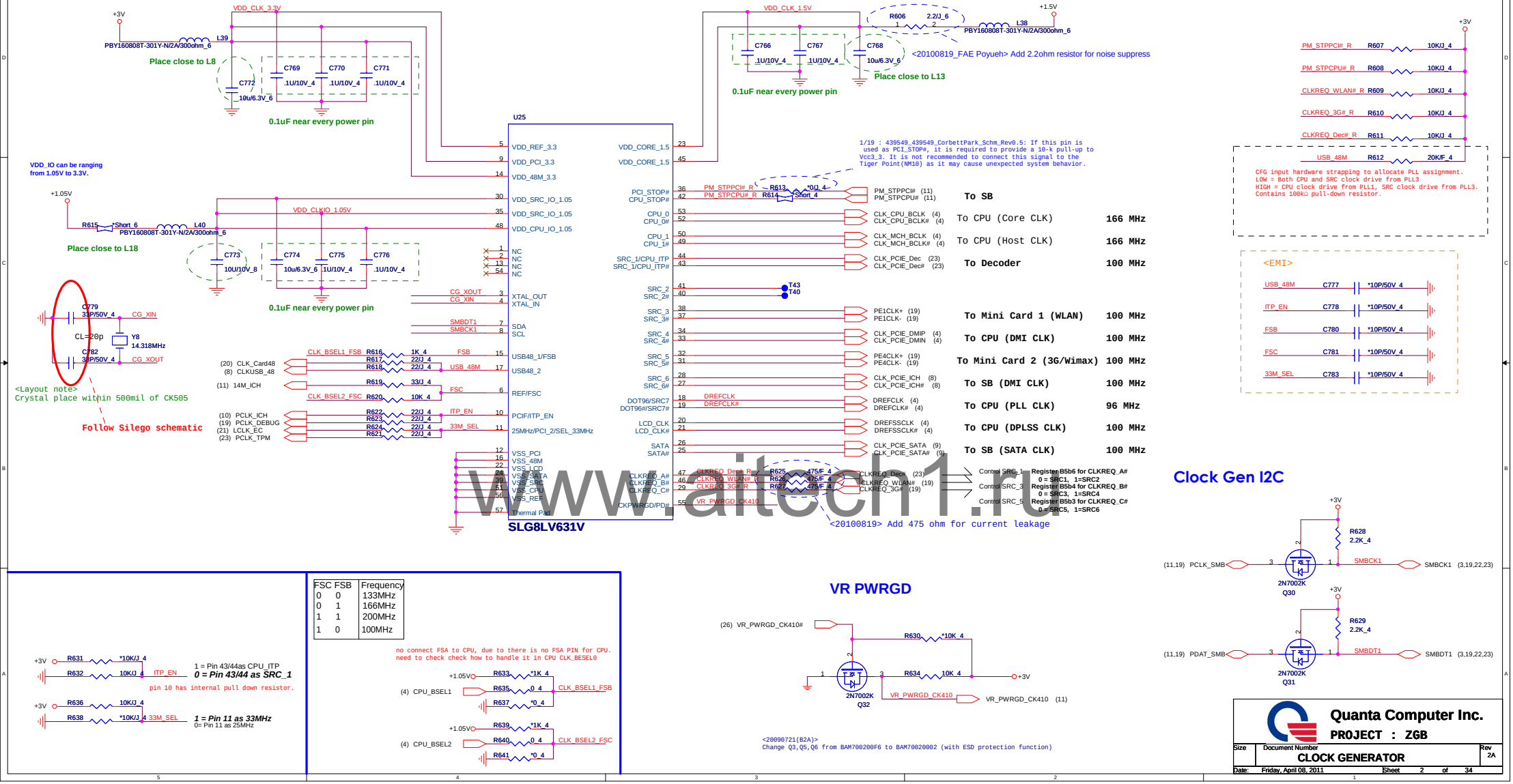
Quanta Computer Inc.
PROJECT : ZGB

Size	Document Number	Rev
	Block Diagram	2A

Date: Friday, April 08, 2011 Sheet 1 of 34

CLK GEN (CLK)

02



Clock Gen I2C

FSC	FSB	Frequency
0	0	133MHz
0	1	166MHz
1	1	200MHz
1	0	100MHz

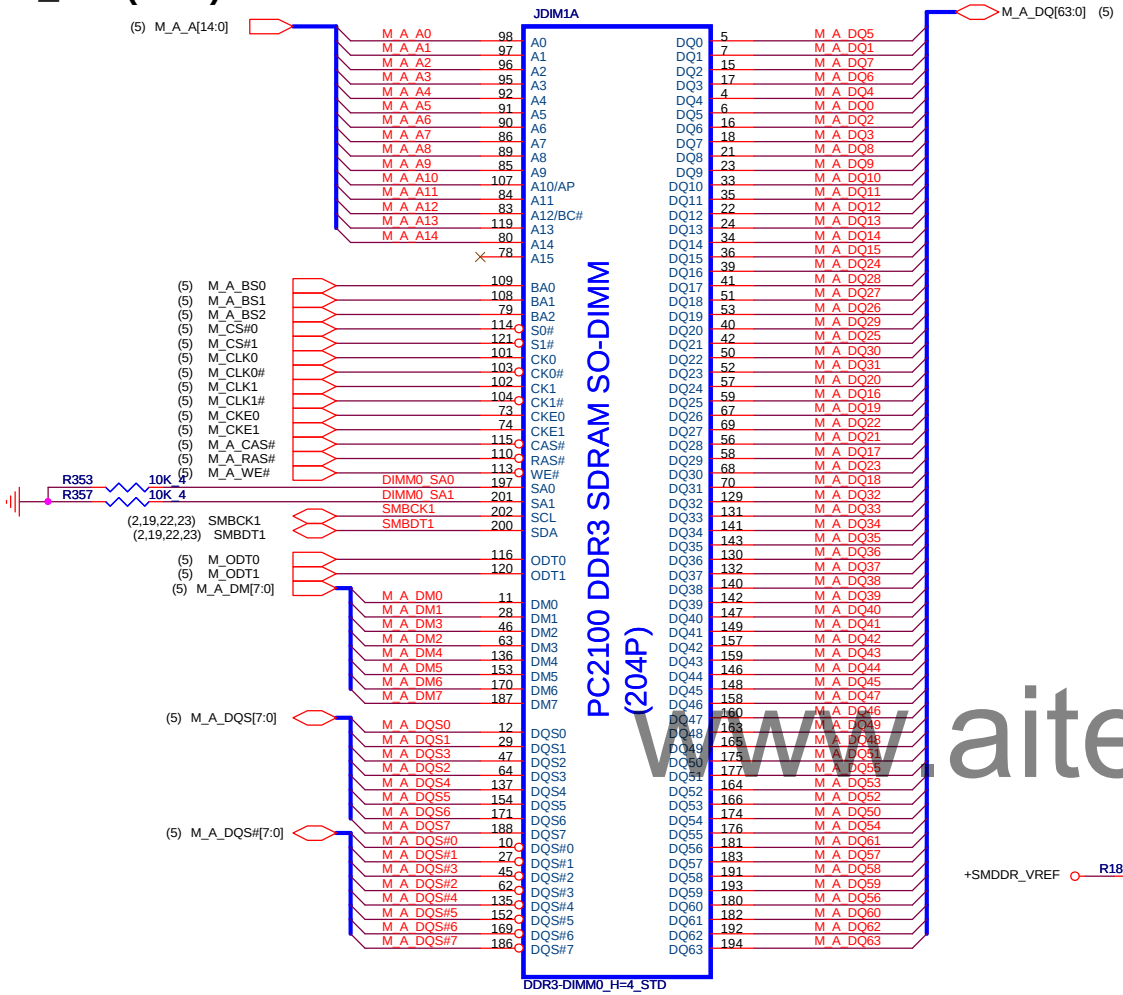
VR PWRGD

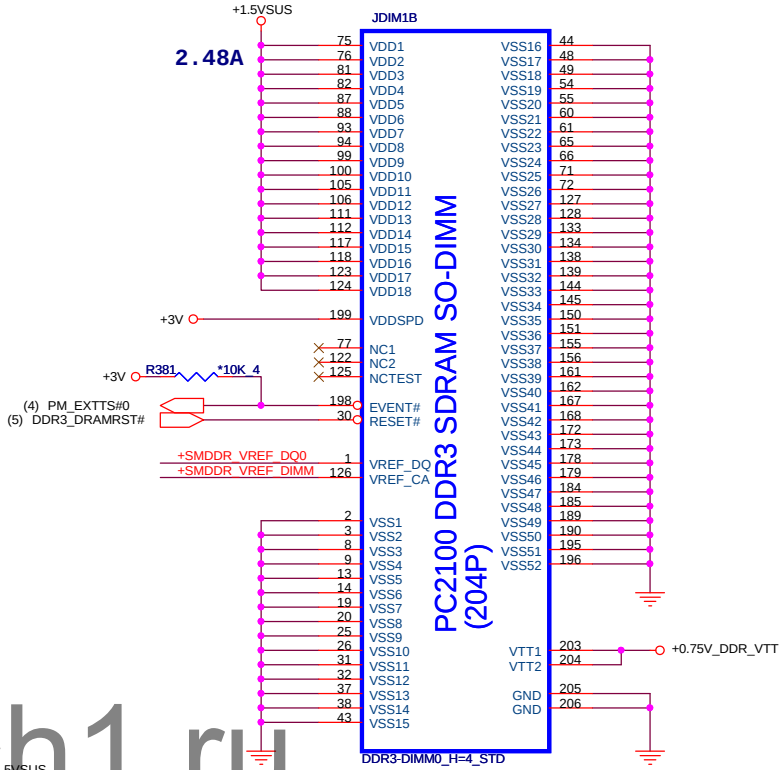
<20090721(B2A)>
Change Q3,Q5,Q6 from BAM700200F6 to BAM70020002 (with ESD protection function)

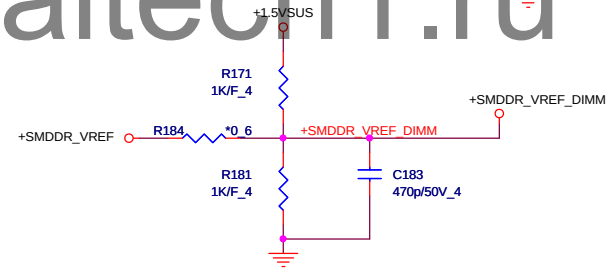
Quanta Computer Inc.
PROJECT : ZGB

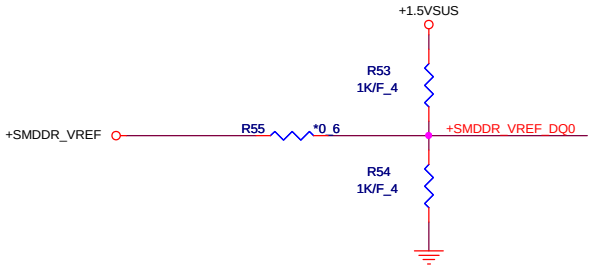
Size	Document Number	Rev
	CLOCK GENERATOR	2A
Date: Friday, April 08, 2011	Sheet 2 of 34	

DDR_STD(DDR)

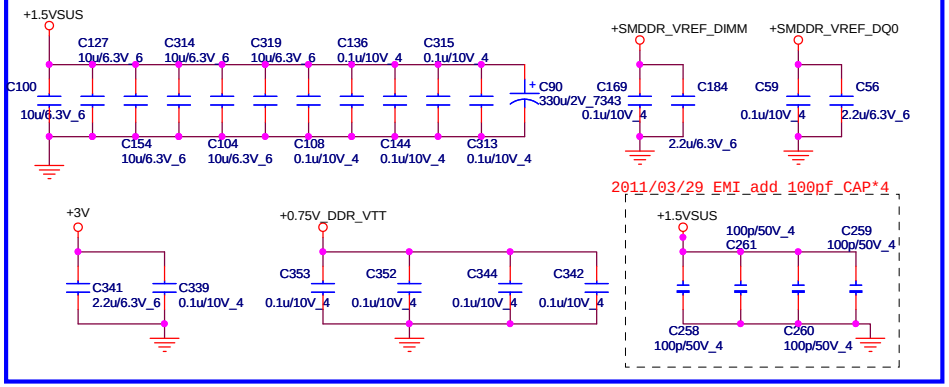








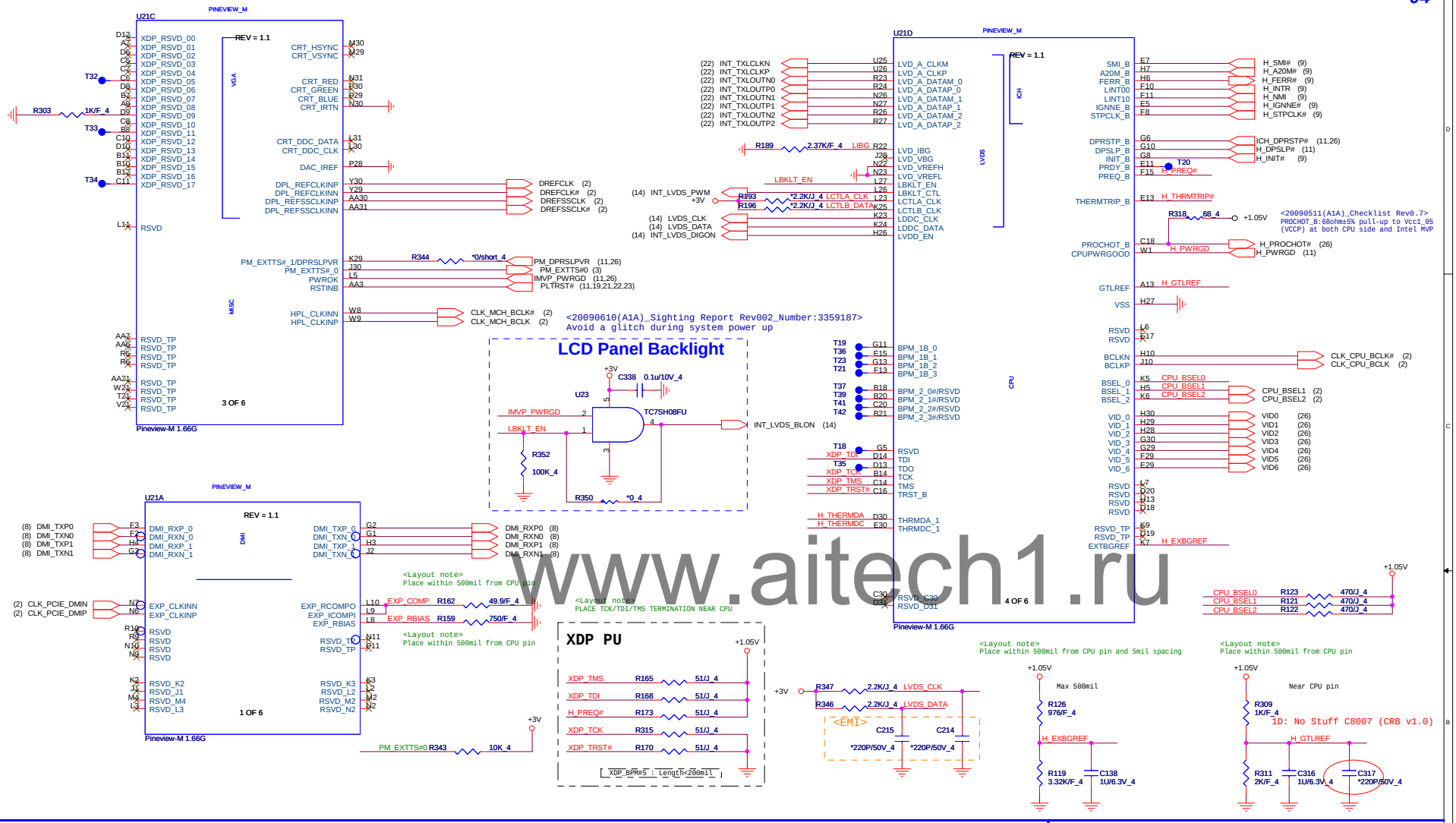
Place these Caps near So-Dimm0.



Quanta Computer Inc.

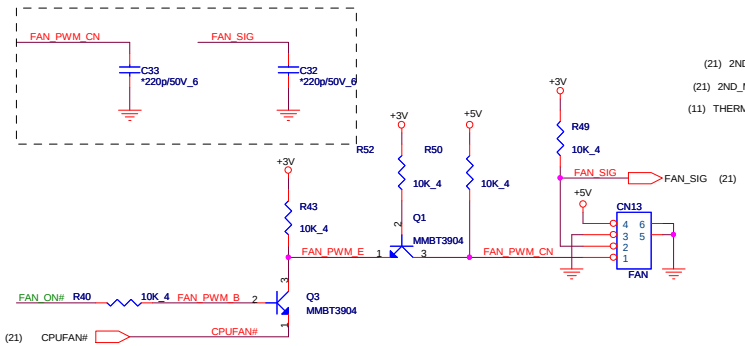
PROJECT : ZGB

Size	Document Number	Rev
	DDRIII SO-DIMM-0	2A
Date: Friday, April 08, 2011	Sheet 3 of 34	

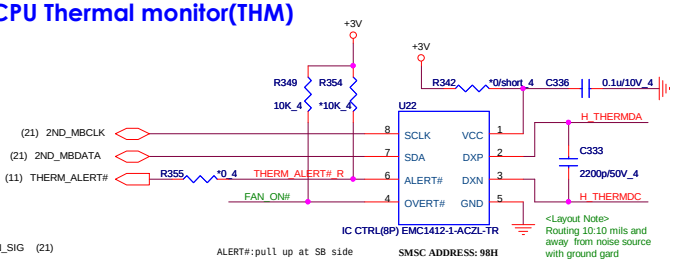


CPU FAN CTRL(THM)

8/11 B-test : for EMI

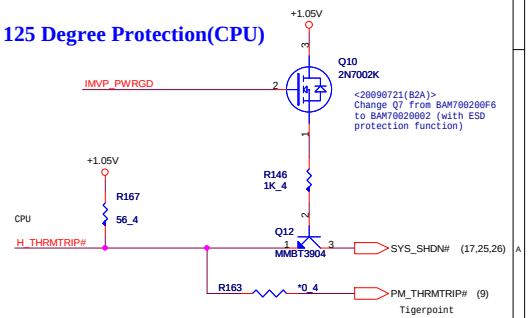


CPU Thermal monitor(THM)



SMSC : AL001412003

125 Degree Protection(CPU)



Quanta Computer Inc.		
PROJECT : ZGB		
Size	Document Number	Rev
	Pineview DMI/Display	2A
Date: Friday, April 08, 2011	Sheet 4 of 34	

PINEVIEW_M

U21B

REV = 1.1

(3) M_A_A[14..0]

M_A_A0 AH19 DDR_A_MA_0
M_A_A1 AJ18 DDR_A_MA_1
M_A_A2 AK18 DDR_A_MA_2
M_A_A3 AK16 DDR_A_MA_3
M_A_A4 AJ14 DDR_A_MA_4
M_A_A5 AH14 DDR_A_MA_5
M_A_A6 AK14 DDR_A_MA_6
M_A_A7 AJ12 DDR_A_MA_7
M_A_A8 AH13 DDR_A_MA_8
M_A_A9 AK12 DDR_A_MA_9
M_A_A10 AK20 DDR_A_MA_10
M_A_A11 AH12 DDR_A_MA_11
M_A_A12 AJ11 DDR_A_MA_12
M_A_A13 AJ24 DDR_A_MA_13
M_A_A14 AJ10 DDR_A_MA_14

(3) M_A_WE#
(3) M_A_CAS#
(3) M_A_RAS#
M_A_WE# AK22 DDR_A_WEB
M_A_CAS# AJ22 DDR_A_CASB
M_A_RAS# AK21 DDR_A_RASB

(3) M_A_BS0
(3) M_A_BS1
(3) M_A_BS2
M_A_BS0 AJ20 DDR_A_BS_0
M_A_BS1 AH20 DDR_A_BS_1
M_A_BS2 AK11 DDR_A_BS_2

(3) M_CS#0
(3) M_CS#1
M_CS#0 AH22 DDR_A_CSB_0
M_CS#1 AK25 DDR_A_CSB_1
AJ21 DDR_A_CSB_2
AJ25 DDR_A_CSB_3

(3) M_CKE0
(3) M_CKE1
M_CKE0 AH10 DDR_A_CKE_0
M_CKE1 AH9 DDR_A_CKE_1
AK10 DDR_A_CKE_2
AJ8 DDR_A_CKE_3

(3) M_ODT0
(3) M_ODT1
M_ODT0 AK24 DDR_A_ODT_0
M_ODT1 AH26 DDR_A_ODT_1
AH24 DDR_A_ODT_2
AK27 DDR_A_ODT_3

(3) M_CLK0
(3) M_CLK0#
(3) M_CLK1
(3) M_CLK1#
M_CLK0 AG15 DDR_A_CK_0
M_CLK#0 AE15 DDR_A_CKB_0
M_CLK1 AD13 DDR_A_CK_1
M_CLK#1 AC13 DDR_A_CKB_1

AC15 DDR_A_CK_2
AD15 DDR_A_CKB_2
AF13 DDR_A_CK_3
AG13 DDR_A_CKB_3

AD17 RSVD_AD17
AC17 RSVD_AC17
AB15 RSVD_AB15
AB17 RSVD_AB17

DDRAM_PWROK AB4 VSS
AK8 RSVD

AB11 RSVD_TP
AB13 RSVD_TP

DDR_VREF AL28 DDR_VREF
AK28 DDR_RPD
AJ26 DDR_RPU

AK29 RSVD

DDR_A

2 OF 6

Pineview-M 1.66G

DDR_A_DQS_0 AD3 M_A_DQS0
DDR_A_DQSB_0 AD2 M_A_DQS#0
DDR_A_DM_0 AD4 M_A_DM0

DDR_A_DQ_0 AC4 M_A_DQ0
DDR_A_DQ_1 AC1 M_A_DQ1
DDR_A_DQ_2 AF4 M_A_DQ2
DDR_A_DQ_3 AG2 M_A_DQ3
DDR_A_DQ_4 AB2 M_A_DQ4
DDR_A_DQ_5 AB3 M_A_DQ5
DDR_A_DQ_6 AE2 M_A_DQ6
DDR_A_DQ_7 AE3 M_A_DQ7

DDR_A_DQS_1 AB8 M_A_DQS1
DDR_A_DQSB_1 AD7 M_A_DQS#1
DDR_A_DM_1 AA9 M_A_DM1

DDR_A_DQ_8 AB6 M_A_DQ8
DDR_A_DQ_9 AB7 M_A_DQ9
DDR_A_DQ_10 AE5 M_A_DQ10
DDR_A_DQ_11 AG5 M_A_DQ11
DDR_A_DQ_12 AA5 M_A_DQ12
DDR_A_DQ_13 AB5 M_A_DQ13
DDR_A_DQ_14 AB9 M_A_DQ14
DDR_A_DQ_15 AD6 M_A_DQ15

DDR_A_DQS_2 AD8 M_A_DQS2
DDR_A_DQSB_2 AD10 M_A_DQS#2
DDR_A_DM_2 AE8 M_A_DM2

DDR_A_DQ_16 AG8 M_A_DQ16
DDR_A_DQ_17 AG7 M_A_DQ17
DDR_A_DQ_18 AE10 M_A_DQ18
DDR_A_DQ_19 AG11 M_A_DQ19
DDR_A_DQ_20 AF7 M_A_DQ20
DDR_A_DQ_21 AF8 M_A_DQ21
DDR_A_DQ_22 AD11 M_A_DQ22
DDR_A_DQ_23 AE10 M_A_DQ23

DDR_A_DQS_3 AK5 M_A_DQS3
DDR_A_DQSB_3 AK3 M_A_DQS#3
DDR_A_DM_3 AJ3 M_A_DM3

DDR_A_DQ_24 AH1 M_A_DQ24
DDR_A_DQ_25 AJ2 M_A_DQ25
DDR_A_DQ_26 AK6 M_A_DQ26
DDR_A_DQ_27 AJ7 M_A_DQ27
DDR_A_DQ_28 AF3 M_A_DQ28
DDR_A_DQ_29 AH2 M_A_DQ29
DDR_A_DQ_30 AL5 M_A_DQ30
DDR_A_DQ_31 AJ6 M_A_DQ31

DDR_A_DQS_4 AG22 M_A_DQS4
DDR_A_DQSB_4 AG21 M_A_DQS#4
DDR_A_DM_4 AD19 M_A_DM4

DDR_A_DQ_32 AE19 M_A_DQ32
DDR_A_DQ_33 AG19 M_A_DQ33
DDR_A_DQ_34 AF22 M_A_DQ34
DDR_A_DQ_35 AD22 M_A_DQ35
DDR_A_DQ_36 AG17 M_A_DQ36
DDR_A_DQ_37 AE19 M_A_DQ37
DDR_A_DQ_38 AF21 M_A_DQ38
DDR_A_DQ_39 AD21 M_A_DQ39

DDR_A_DQS_5 AE26 M_A_DQS5
DDR_A_DQSB_5 AG27 M_A_DQS#5
DDR_A_DM_5 AJ27 M_A_DM5

DDR_A_DQ_40 AE24 M_A_DQ40
DDR_A_DQ_41 AG25 M_A_DQ41
DDR_A_DQ_42 AD25 M_A_DQ42
DDR_A_DQ_43 AD24 M_A_DQ43
DDR_A_DQ_44 AC22 M_A_DQ44
DDR_A_DQ_45 AG24 M_A_DQ45
DDR_A_DQ_46 AD27 M_A_DQ46
DDR_A_DQ_47 AE27 M_A_DQ47

DDR_A_DQS_6 AE30 M_A_DQS6
DDR_A_DQSB_6 AE29 M_A_DQS#6
DDR_A_DM_6 AE30 M_A_DM6

DDR_A_DQ_48 AG31 M_A_DQ48
DDR_A_DQ_49 AG30 M_A_DQ49
DDR_A_DQ_50 AD30 M_A_DQ50
DDR_A_DQ_51 AD29 M_A_DQ51
DDR_A_DQ_52 AJ30 M_A_DQ52
DDR_A_DQ_53 AJ29 M_A_DQ53
DDR_A_DQ_54 AE29 M_A_DQ54
DDR_A_DQ_55 AD28 M_A_DQ55

DDR_A_DQS_7 AB27 M_A_DQS7
DDR_A_DQSB_7 AA27 M_A_DQS#7
DDR_A_DM_7 AB26 M_A_DM7

DDR_A_DQ_56 AA24 M_A_DQ56
DDR_A_DQ_57 AB25 M_A_DQ57
DDR_A_DQ_58 W24 M_A_DQ58
DDR_A_DQ_59 W22 M_A_DQ59
DDR_A_DQ_60 AB24 M_A_DQ60
DDR_A_DQ_61 AB23 M_A_DQ61
DDR_A_DQ_62 AA23 M_A_DQ62
DDR_A_DQ_63 W27 M_A_DQ63

M_A_DQ[63..0] (3)
M_A_DM[7..0] (3)
M_A_DQS[7..0] (3)
M_A_DQS#[7..0] (3)

DDR3 PWROK

+3V_S5

(21,27,29) SUSON
(21,27) HWPG_1.5V

U9
TC7SH08FU

R142 12.1K/F_4
DDRAM_PWROK
R143 10K_4

(3) DDR3_DRAMRST#
+1.5VSUS
R296 *10K_4

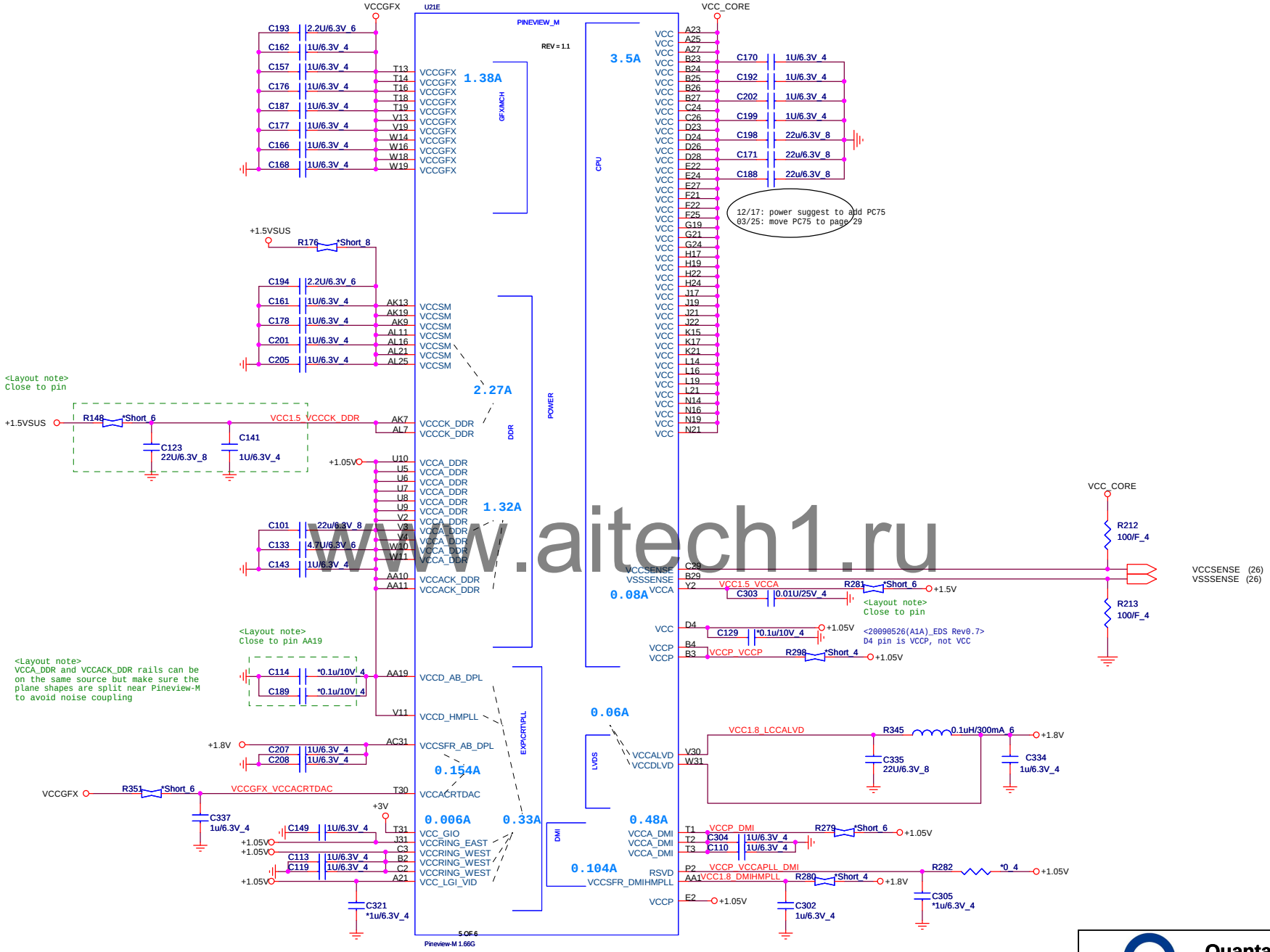
<Layout note>
Close to pin
C329 0.1U/10V_4
R339 80.6/F_4 SM_RCOMP
R323 80.6/F_4 SM_RCOMP#
C322 0.01U/25V_4

+1.5VSUS
<Layout note>
Close to DDR_VREF pin
R325 1K/F_4
+SMDDR_VREF
R330 *0_4 DDR_VREF
R335 1K/F_4
C330 0.1u/16V_6
<EMI>
C324 *1000p/50V_4

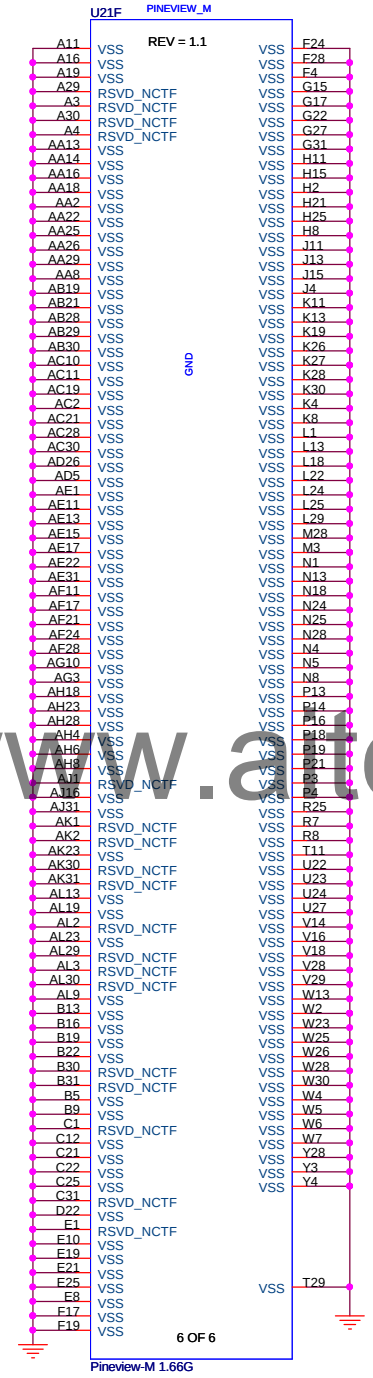
DG 2.1 : It is strongly recommended that the SODIMM VREF motherboard traces, going from their VREF resistor dividers to their specified SODIMM VREF pins, be ground referenced on the motherboard where ever possible to help minimize risks of any possible noise being coupled onto VREF. If they can't be referenced to ground we recommend placing a site for a 0603 capacitor near the VREF divider. These 0603 capacitor sites must be connected on one end to the non ground reference plane the VREF trace is referenced to and the other end must be connected to ground.

Quanta Computer Inc.
PROJECT : ZGB

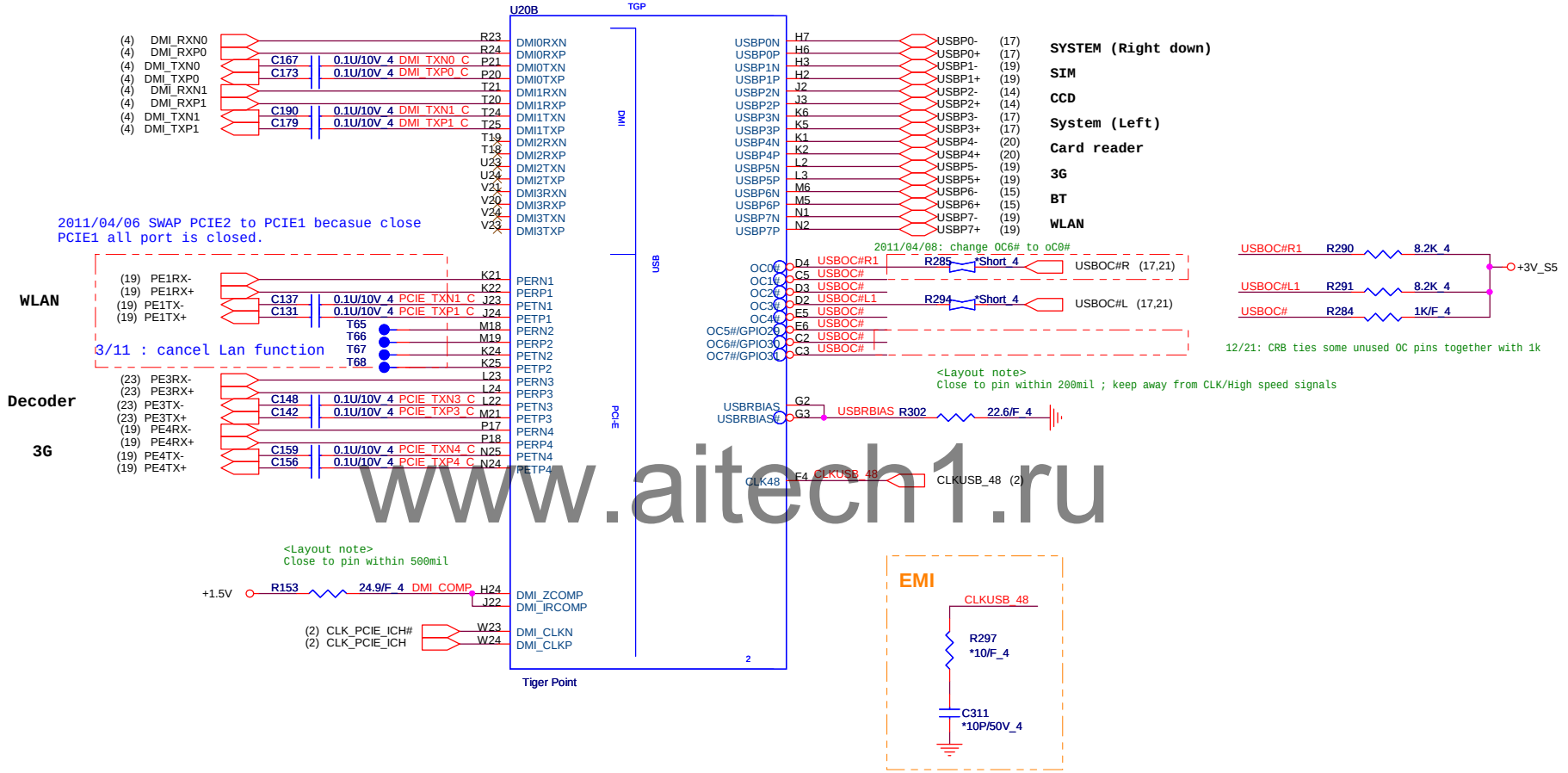
Size	Document Number	Rev
	Pineview DDR	2A
Date: Friday, April 08, 2011	Sheet 5 of 34	



Quanta Computer Inc.		
PROJECT : ZGB		
Size	Document Number: Pineview Power	Rev: 2A
Date: Friday, April 08, 2011	Sheet 6 of 34	



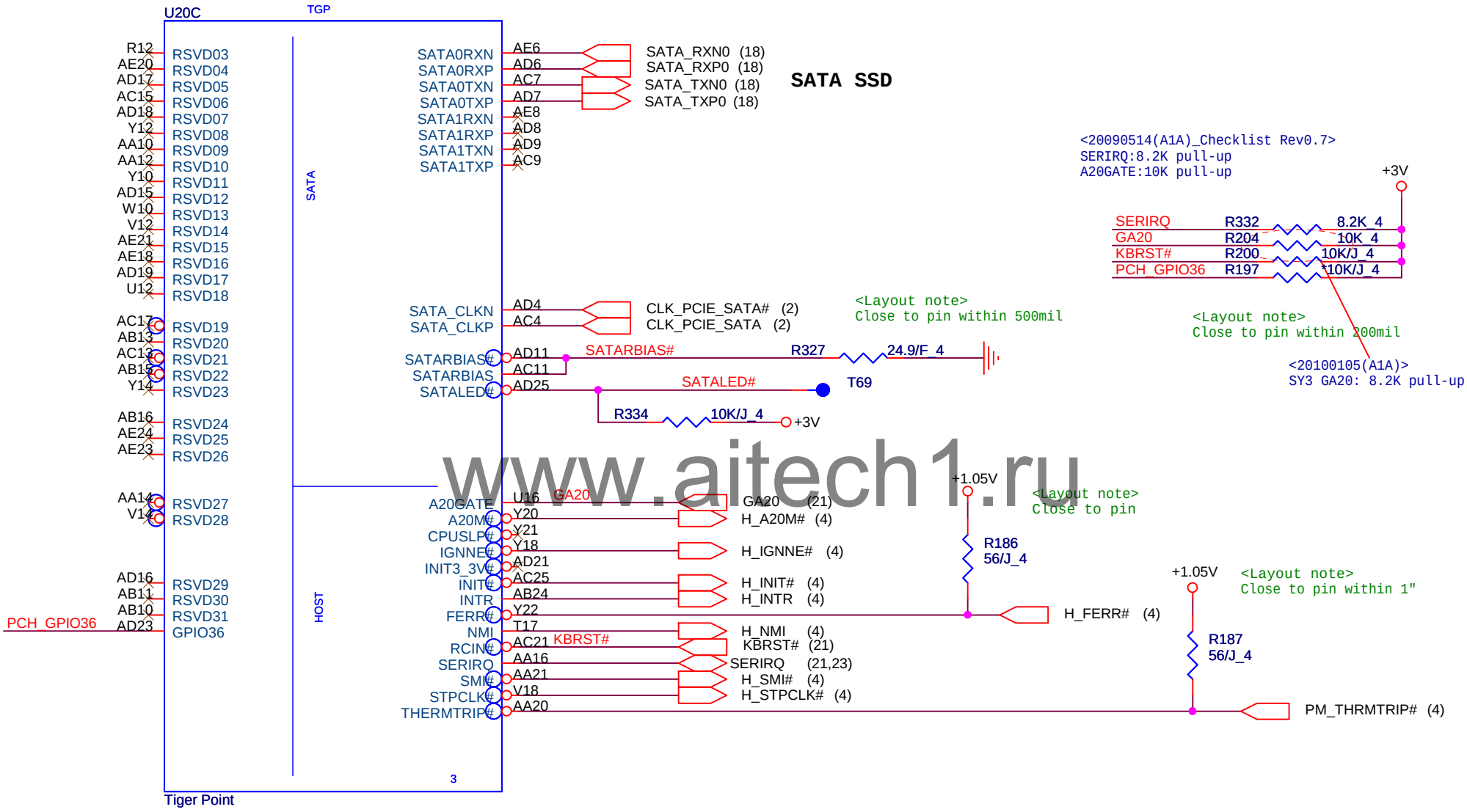
Quanta Computer Inc.		
PROJECT : ZGB		
Size	Document Number: Pineview GND	Rev: 2A
Date: Friday, April 08, 2011	Sheet 7 of 34	



Quanta Computer Inc.

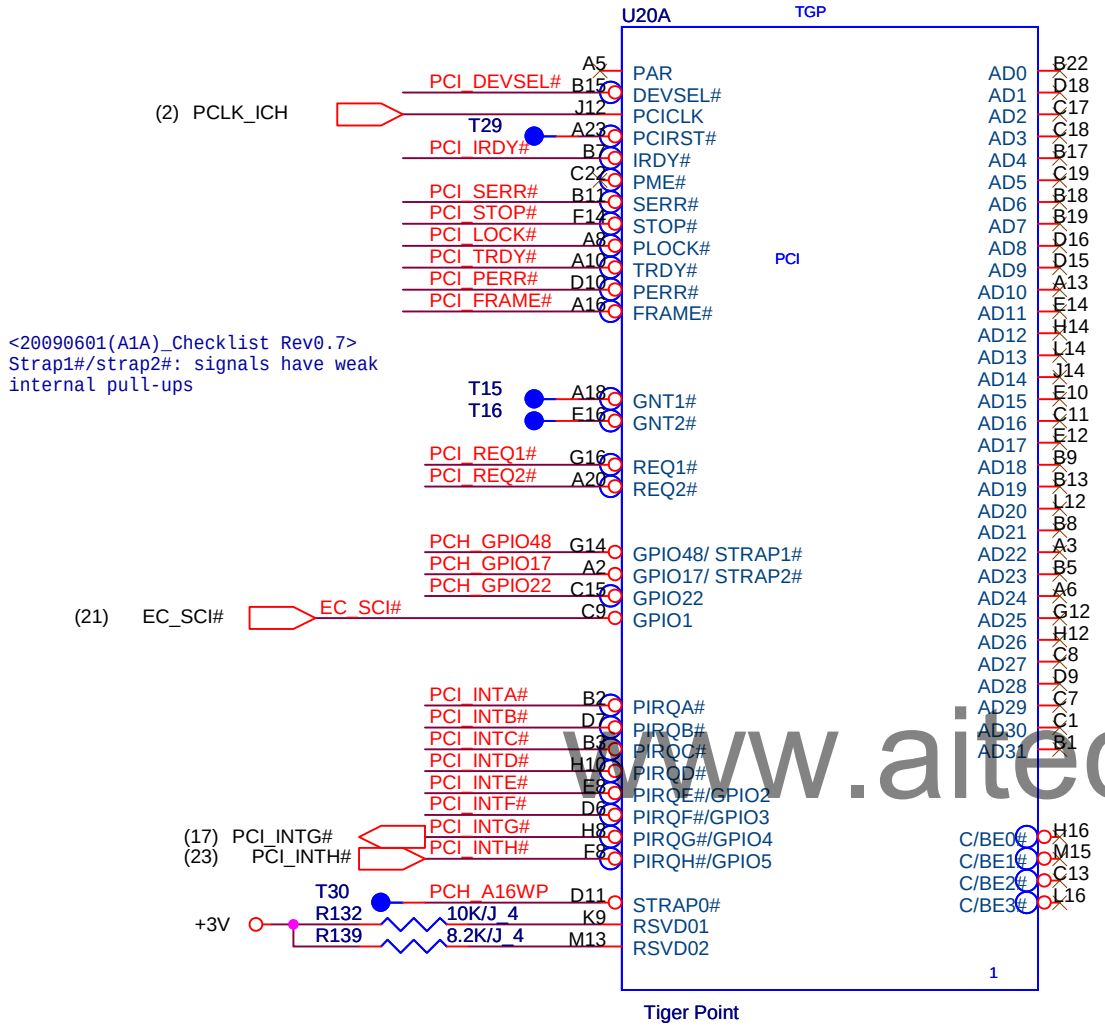
PROJECT : ZGB

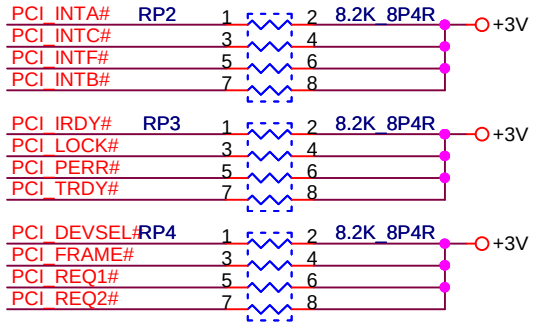
Size	Document Number	Rev
	Tiger Point DMI/PCIE/USB	2A
Date: Friday, April 08, 2011	Sheet 8 of 34	



NOTE :
1. CPUSLP# is supported only on nettop platforms.

Quanta Computer Inc.		
PROJECT : ZGB		
Size	Document Number: Tiger Point Sata/Host	Rev: 2A
Date: Friday, April 08, 2011	Sheet 9 of 34	





IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 Codec; option for SMBUS
PIRQC	USB UH Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCI, TCO, HPET#0,1,2
PIRQF	Option for SCI, TCO, HPET#0,1,2
PIRQG	Option for SCI, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2

PCI_GNT#2	Internal PU Should not be PD

ICH Boot BIOS select

PCH_GPIO17 (INT PU)	PCH_GPIO48 (INT PU)	Boot BIOS Location
0	1	SPI **(Default)**
1	0	PCI
1	1	LPC

A16 SWAP Override strap

PCH_A16WP (INT PU)	**Low = A16 swap override enabled** **High = Default**

Quanta Computer Inc.

PROJECT : ZGB

Size	Document Number	Rev
	TigerPoint PCI(3/6)	2A
Date: Friday, April 08, 2011	Sheet 10 of 34	

EMI

14M_ICH
R320 *33/J_4
C323 *10P/50V_4

debug port for google require

D23,D24 are just for preventing EC/SB F/W error to cause to leakage current.If test OK, they can be connected directly.

<20090515(A1A)_Checklist Rev0.7>
BATLOW#:8.2K pull-up to V3ALWAYS
WAKE#:10K pull-up to VccSus3_3
SYS_RST#:10K pull-up to VccSus3_3

U20D TGP

LPC: LAD0/FWH0, LAD1/FWH1, LAD2/FWH2, LAD3/FWH3, LDRQ0#, LFRAME#
AUDIO: HDA_BIT_CLK, HDA_RST#, HDA_SDI0, HDA_SDIN1, HDA_SDIN2, HDA_SDOUT, HDA_SYNC, CLK14
EEPROM: EE_CS, EE_DIN, EE_DOUT, EE_SHCLK
LAN: LAN_CLK, LANR_STSYNC, LAN_RST#, LAN_RXD0, LAN_RXD1, LAN_RXD2, LAN_TXD0, LAN_TXD1, LAN_TXD2
RTC: RTCX1, RTCX2, RTCRST#
SMB: SMBALERT#/GPIO11, SMBCLK, SMBDATA, SMLALERT#, SMLINK0, SMLINK1
SPI: SPI_MISO, SPI_MOSI, SPI_CS#, SPI_CLK, SPI_ARB
MISC: BM_BUSY#/GPIO0, GPIO6, GPIO7, GPIO8, GPIO9, GPIO10, GPIO12, GPIO13, GPIO14, GPIO15, DPRSLPVR, STP_PCI#, STP_CPU#, GPIO24, GPIO25, GPIO26, GPIO27, GPIO28, CLKRUN#, GPIO33, GPIO34, GPIO38, GPIO39, CPUPWRGD/GPIO49, THRM#, VRMPWRGD, MCH_SYNC#, PWRBTN#, RI#, SUS_STAT#/LPCPD#, SUSCLK, SYS_RESET#, PLTRST#, WAKE#, INTRUDER#, PWROK, RSMRST#, INTVRMEN, SPKR, SLP_S3#, SLP_S4#, SLP_S5#, BATLOW#, DPRSTP#, DPSLP#, RSVD31

T24 AA5 LDRQ1#/GPIO23
(19,21,23) LPCAD0 V6 LAD0/FWH0
(19,21,23) LPCAD1 AA6 LAD1/FWH1
(19,21,23) LPCAD2 V5 LAD2/FWH2
(19,21,23) LPCAD3 W8 LAD3/FWH3
T25 Y8 LDRQ0#
(19,21,23) LPCFRAME# Y4 LFRAME#

(16) ACZ_BITCLK_AUDIO R160 33/J_4 ACZ_BITCLK_R P6 HDA_BIT_CLK
(16) ACZ_RESET#_AUDIO R161 33/J_4 ACZ_RST#_R U2 HDA_RST#
(16) ACZ_SDIN0 W2 HDA_SDI0
V2 HDA_SDIN1
P8 HDA_SDIN2
(16) ACZ_SDOUT_AUDIO R185 33/J_4 ACZ_SDOUT_R AA1 HDA_SDOUT
(16) ACZ_SYNC_AUDIO R175 33/J_4 ACZ_SYNC_R Y1 HDA_SYNC
(2) 14M_ICH AA3 CLK14

U3 EE_CS
AE2 EE_DIN
T6 EE_DOUT
V3 EE_SHCLK

T4 LAN_CLK
P2 LANR_STSYNC
B23 LAN_RST#
AA2 LAN_RXD0
AD1 LAN_RXD1
AC2 LAN_RXD2
W3 LAN_TXD0
T1 LAN_TXD1
U4 LAN_TXD2

C318 15P/50V_4
Y3 32.768K/10PPM
C320 15P/50V_4
R319 10M/J_4
RTC_X1 W4 RTCX1
RTC_X2 V5 RTCX2
RTCRST# T5 RTCRST#

<20090529(A1A)_Checklist Rev0.7>
If integrated LAN is not used
LAN_RST# tie it to GND.

SMBALERT# E20 SMBALERT#/GPIO11
(2,19) PCLK_SMB H18 SMBCLK
(2,19) PDAT_SMB E23 SMBDATA
SMB_LINK_ALERT# H21 SMLALERT#
SMLINK0 F25 SMLINK0
SMLINK1 F24 SMLINK1

SPI_MISO R2 SPI_MISO
SPI_MOSI T1 SPI_MOSI
SPI_CS# M8 SPI_CS#
SPI_CLK P9 SPI_CLK
T22 R4 SPI_ARB

BM_BUSY#/GPIO0 T15 BM_BUSY#
GPIO6 W16 RECOVER_KEY#_R1 — D24 BAS316 — RECOVER_KEY#_R (17,21)
GPIO7 W14 DEVELOPER#_R1 — D23 BAS316 — DEVELOPER#_R (17,21)
GPIO8 K18 EC_SMI# — EC_SMI# (17,21)
GPIO9 H19 LID#_ICH — D21 BAS316 — LID# (14,17,21)
GPIO10 M17 MANU_0_4 — R118 — MANU_SW_TPT (21)
GPIO12 A24 SINT_TP
GPIO13 C23 MBID1
GPIO14 P5 MBID0
GPIO15 E24 HDMI_CON_HP_TP — HDMI_CON_HP_TP (22)
DPRSLPVR AB20 — PM_DPRSLPVR (4,26)
STP_PCI# Y16 — PM_STPPCI# (2)
STP_CPU# AB19 — PM_STPCPU# (2)
GPIO24 R3 PCH_GPIO24 — PCH_GPIO24 (17)
GPIO25 C24 DMI_AC_ENABLE
GPIO26 D19 HINT_TP — T51
GPIO27 D20 PCH_GPIO27 — T46
GPIO28 F22 PCH_GPIO28 — T47
CLKRUN# AC19 CLKRUN# — CLKRUN# (21,23) — T48
GPIO33 U14 PCH_GPIO33 — T49
GPIO34 AC1 PCH_GPIO34 — T50
GPIO38 AC23 PCH_GPIO38 — T45
GPIO39 AC24 PCH_GPIO39
CPUPWRGD/GPIO49 AB22 — H_PWRGD (4)
THRM# AB17 — THERM_ALERT# (4)
VRMPWRGD V16 — VR_PWRGD_CK410 (2)
MCH_SYNC# AC18 MCH_SYNC#
PWRBTN# E21 DNBSWON# — DNBSWON# (21)
RI# H23 ICH_RI#
SUS_STAT#/LPCPD# G22 TPM_LPCPD# — TPM_LPCPD# (23)
SUSCLK D22 SUSCLK — SUSCLK (21)
SYS_RESET# G18 SYS_RST#
PLTRST# G23 PLT_RST#
WAKE# C25 PCIE_WAKE# — PCIE_WAKE# (19)
INTRUDER# T8 SM_INTRUDER# — R164 1M/F_6 — VCCRTC
PWROK U10 TPT_PWROK
RSMRST# AC3 EC_RSMRST# — EC_RSMRST# (21)
INTVRMEN AD3 ICH_INTVRMEN — R328 332K/F_4
SPKR J16 — SB_BEEP (16)
SLP_S3# H20 — SUSB# (21)
SLP_S4# E25 — SUSC# (21)
SLP_S5# F21 — T17
BATLOW# B25 PM_BATLOW#
DPRSTP# AB23 — ICH_DPRSTP# (4,26)
DPSLP# AA18 — H_DPSLP# (4)
RSVD31 F20

1C: Intel suggestion enable AC mode

+3V_S5
PCLK_SMB R130 2.2K_4
PDAT_SMB R127 2.2K_4
PM_BATLOW# R273 8.2K_4
THERM_ALERT# R188 8.2K_4
DNBSWON# R117 *10K_4
LID# ICH R150 8.2K_4
EC_SMI# R154 10K_4
SYS_RST# R115 10K_4
SMBALERT# R129 10K_4
SMB_LINK_ALERT# R128 10K_4
PCIE_WAKE# R274 10K_4
SMLINK1 R276 10K_4
SMLINK0 R277 10K_4
HDMI_CON_HP_TP R272 *8.2K_4
ICH_RI# R116 10K_4

+3V
RECOVER_KEY#_R1 R182 1K/F_4
DEVELOPER#_R1 R183 8.2K_4
MCH_SYNC# R331 1K/F_4
CLKRUN# R333 8.2K_4
BM_BUSY# R195 8.2K_4

DMI_AC_ENABLE R275 1K_4
TPT_PWROK R172 10K_4
EC_RSMRST# R190 10K_4

+3V R151 10K_4 SPI_CS#
R308 10K_4 SPI_MISO
R312 10K_4 SPI_MOSI_R
place near to Tiger point.

SPI FLASH(CLG)

(17) SPI_MISO_R — R307 49.9/F_4 — SPI_MISO_R — U11 SO
(17) SPI_MOSI — SPI_MOSI — SI
(17) SPI_CLK — SPI_CLK — SCK
+3V_deg R152 10K_4 SPI_CS# — CE
(17) SPI_CS#
VDD, HOLD, WP, VSS
W25Q32BVSSIG

+3V_deg D34 RSX101M-30 — +3V
R120 3.3K_4 — MANU_SW_R1
C96 .1u/10V_4
2011/04/06 change power plant to +3V_deg.
+3V_deg
R438 100K/F_4

SPI_MOSI R310 49.9/F_4 SPI_MOSI_R
SPI_CS# R361 49.9/F_4 SPI_CS#_R
SPI_CLK R305 49.9/F_4 SPI_CLK_R
T22

2011/04/06 change power plant to +3V_deg.

MANU_SW_R1 — D26 BAS316 — MANU_SW_R (17,21)
2011/04/07 change power plant to +3V_deg.

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

for ZGA use:
Winbond W25Q32BVSSIG AKE391P0N00
MXIC MX25L3205DM2I-12G AKE39FP0Z00

<20090721(B2A)>
Stuff U19 and C275 and un-stuff R205 for power sequence

+3V_S5
R359 10K_4
R271 10K_4
R304 10K_4
MBID1
MBID0
SINT_TP
R262 *10K_4
R270 *10K_4
R306 *10K_4

RTC(RTC)

+3VPCU — D30 CH500H-40 — VCCRTC — C332 1u/10V_6
VCCRTC_3 — D31 CH500H-40 — R338 20K/F_6 — RTCRST# — G3
C331 1u/10V_6
*SHORT_PAD
R348 1K_4
CN22 RTC SOCKET

20MIL
20MIL
+5V_S5
VCCRTC_4 — Q26 MMBT3904 — VCCRTC_1 — R415 4.7K_4 — VCCRTC_2 — R422 4.7K_4
R421 68.1K/F_4
R414 150K/F_4

Platform Reset

+3V — R211 4.7K_4 — U19
C299 0.1u/10V_4
PLT_RST# — TC7SH08FU
(17) DEG_RST#
PLTRST# (4,19,21,22,23)
R286 100K_4
R283 *0_4

<2011/04/07>
Stuff U19 and C299 and un-stuff R283 follow up Intel CRB.
2011/4/8
add U19 pin1 to Deg_RST# from debug port.

TPT Power OK

+3V — C209 *0.1u/10V_4 — U14 *TC7SH08FU
(21) HWPG
(4,26) IMVP_PWRGD
TPT_PWROK
R207 *0/short_4
(21) ECPWROK — R205 *0_4

ACZ_SDOUT (INT PD)	ACZ_SYNC (INT PD)	Description
0	0	* 4 x 1s
1	0	Reserved
0	1	Reserved
1	1	1 x 4s(1 port/4 lanes)

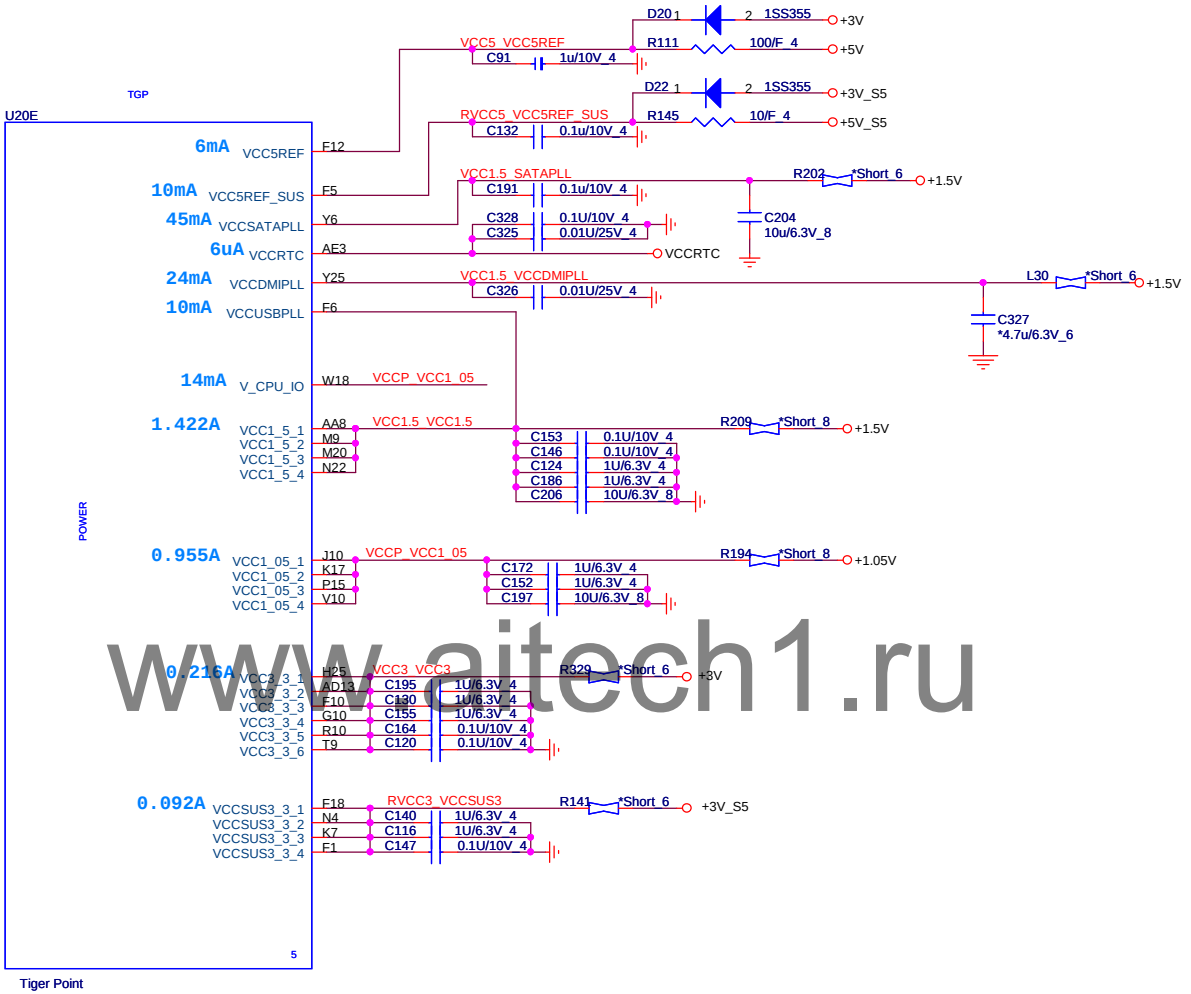
INTVRMEN	
1	Enable internal VccSus1_5 VRM (default)
0	Disable

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZGB

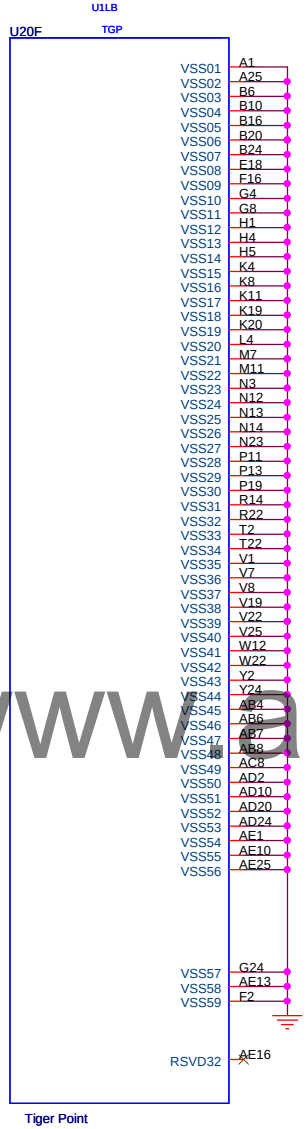
Size	Document Number	Rev
	TigerPoint GPIO	2A
Date: Friday, April 08, 2011	Sheet 11 of 34	

<Layout note>
Place 0402 caps close to ball
Place 0603/0805 caps close to ICH



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

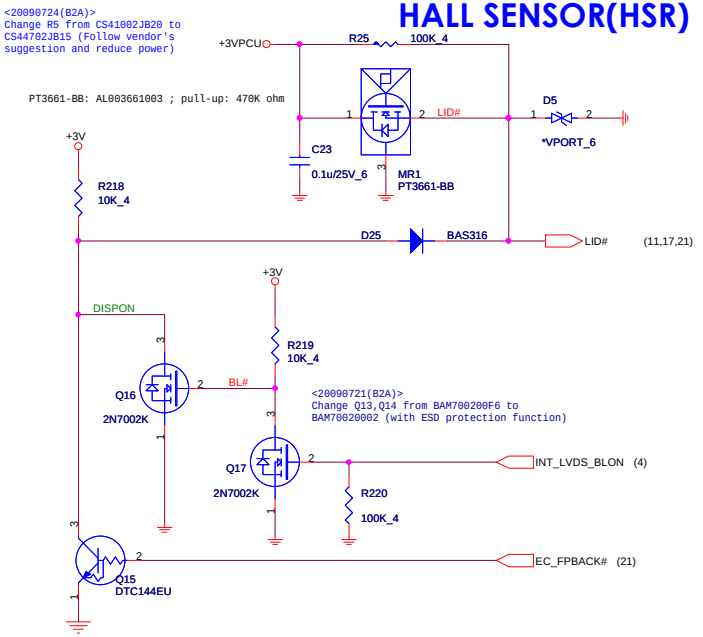
Quanta Computer Inc.		
PROJECT : ZGB		
Size	Document Number: TigerPoint Power	Rev: 2A
Date: Friday, April 08, 2011	Sheet 12 of 34	



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

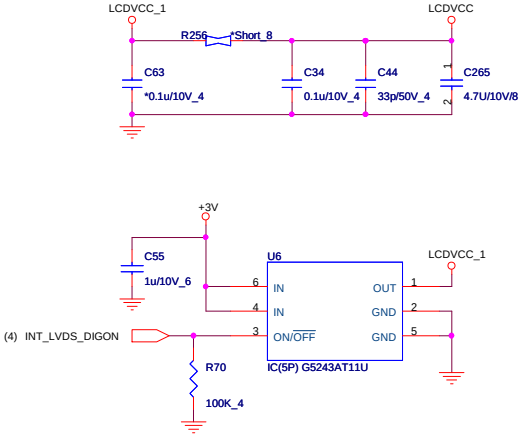
Quanta Computer Inc.		
PROJECT : ZGB		
Size	Document Number: TigerPoint GND	Rev: 2A
Date: Friday, April 08, 2011	Sheet 13 of 34	

HALL SENSOR(HSR)



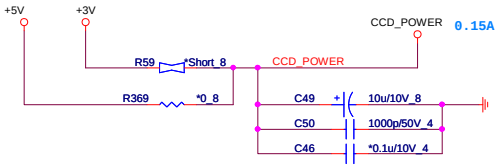
LED Panel POWER SWITCH(LDS)

Irush=1.5A

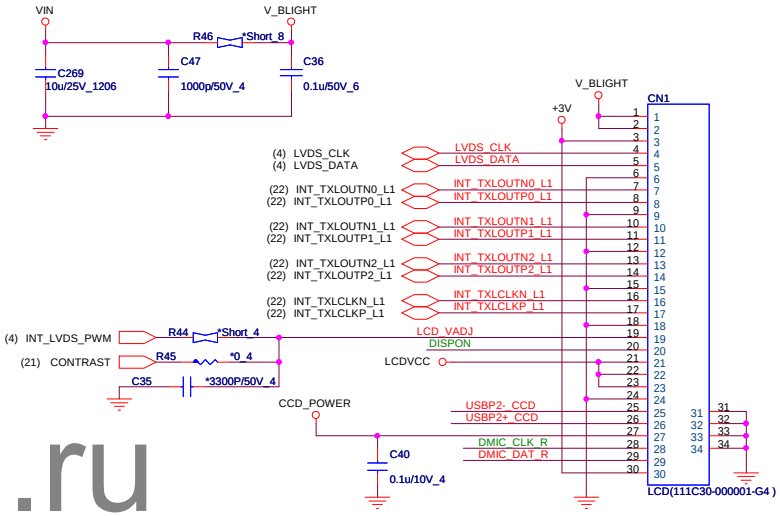


CAMERA POWER(CCD)

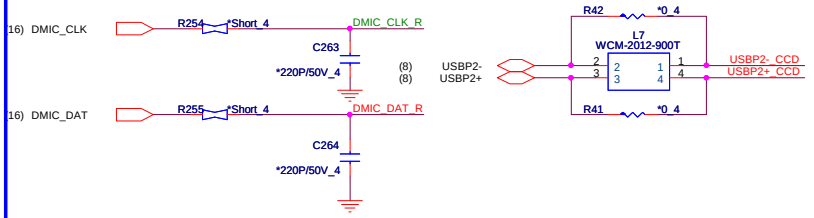
14



LED Panel(LDS)



B-test 8/11: for EMI



CRT(CRT)

3/11 : cancel CRT function

Quanta Computer Inc.

PROJECT : ZGB

Size	Document Number	Rev
	CRT/LVDS	2A

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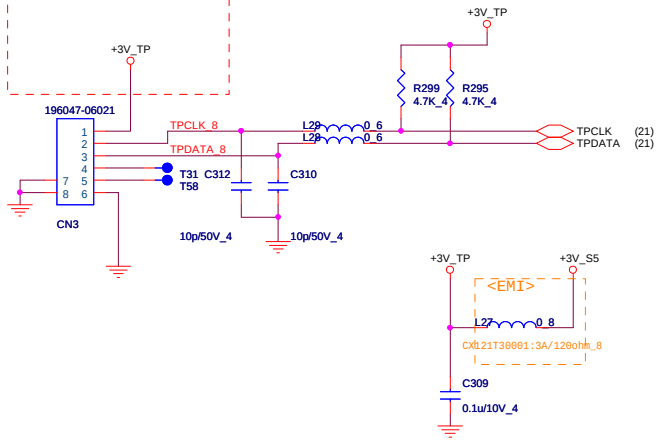
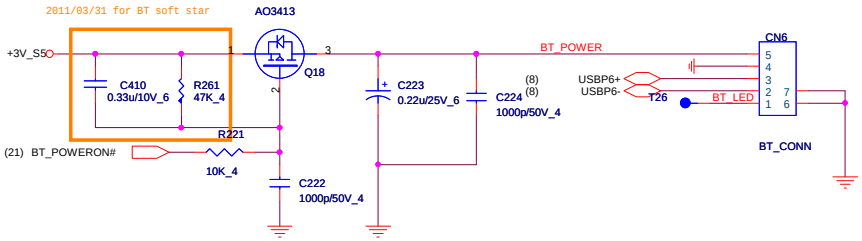
TOUCH PAD(TPD)

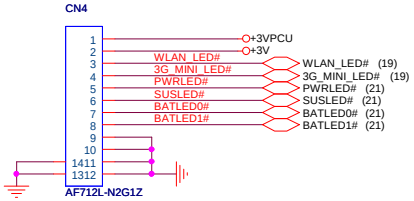
2011/3/28 Remove 4pin connector



BLUETOOTH(BTM)



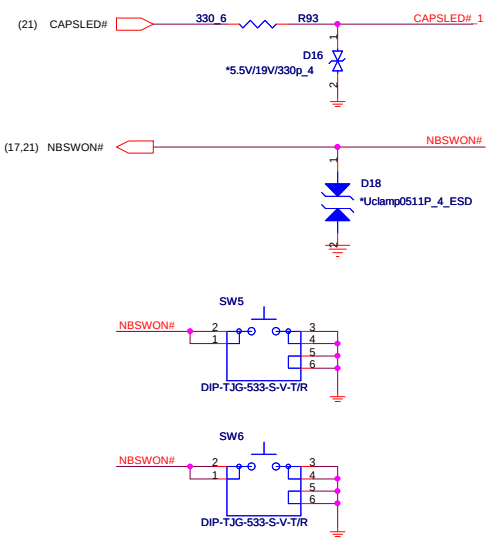
Connector (UIF)



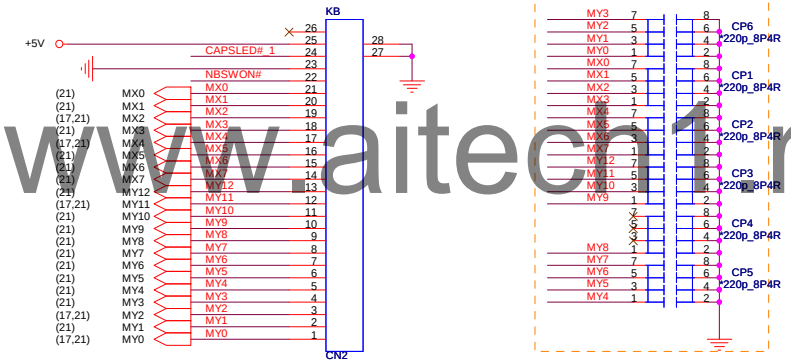
TOUCH PAD I2C(TPD)

2011/3/28 Remove I2C function.

KEYBOARD(KBC)



place on top and botton for A2 test



use key matrix to power on, so,
need to add two pin for NBSWON# and GND

Quanta Computer Inc.
PROJECT : ZGB

Size	Document Number	Rev
	KB/BT/TP/LED/Power Connector	2A

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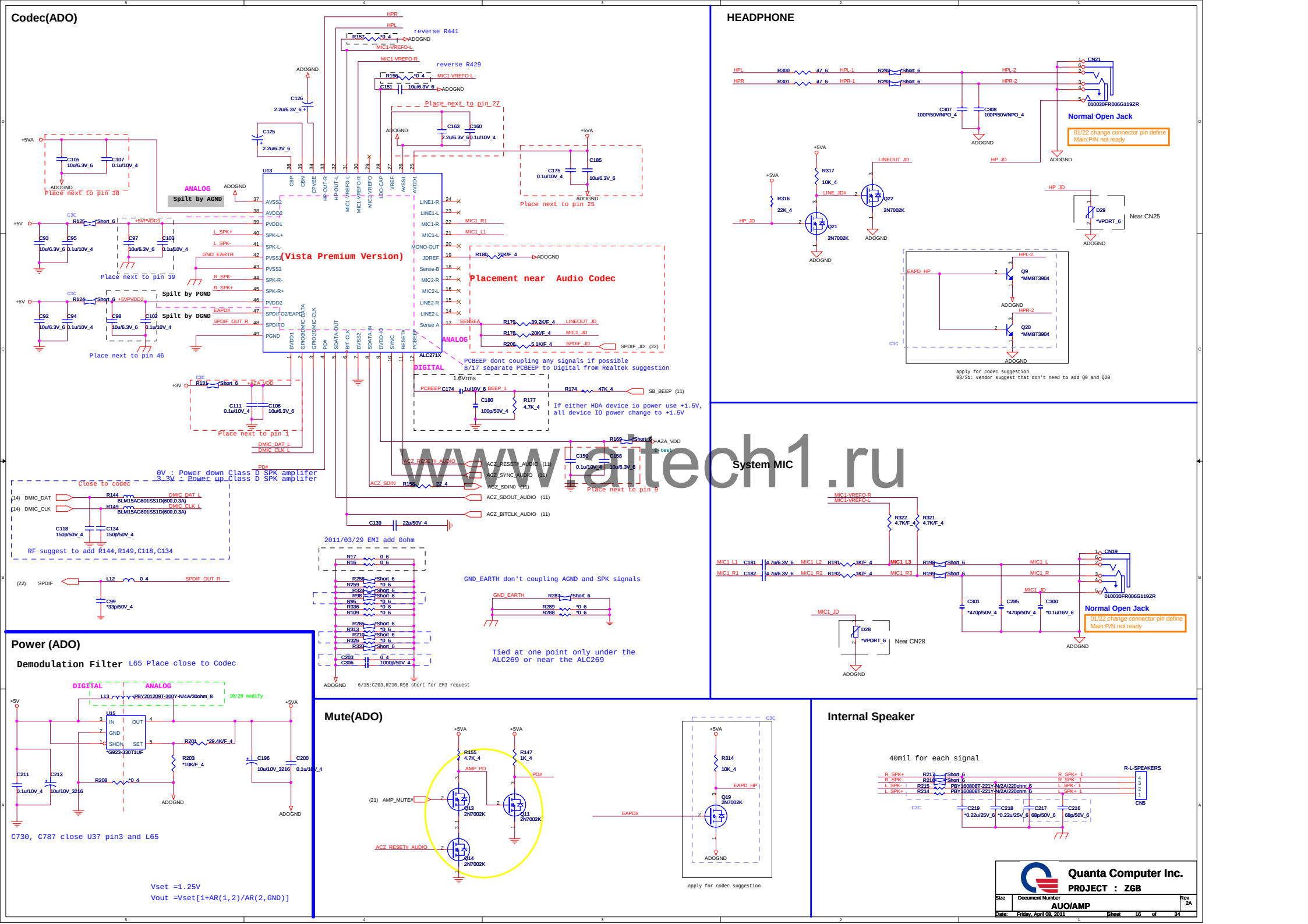
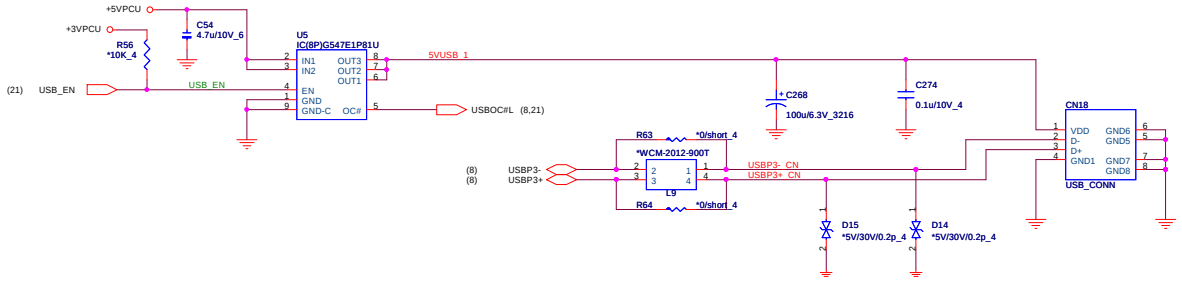
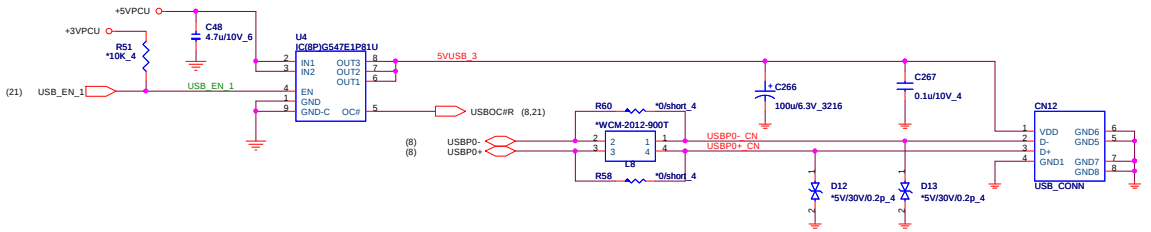
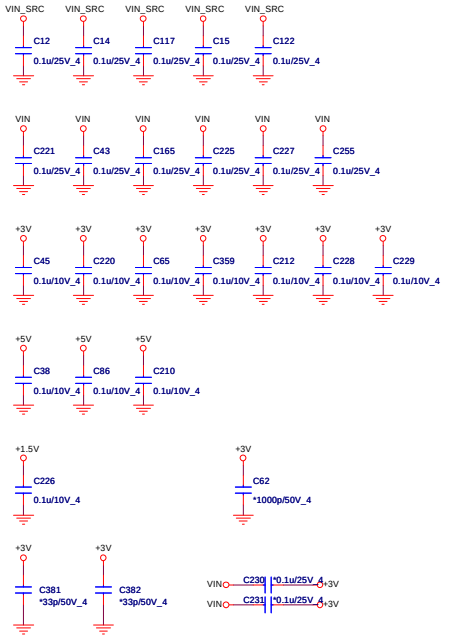
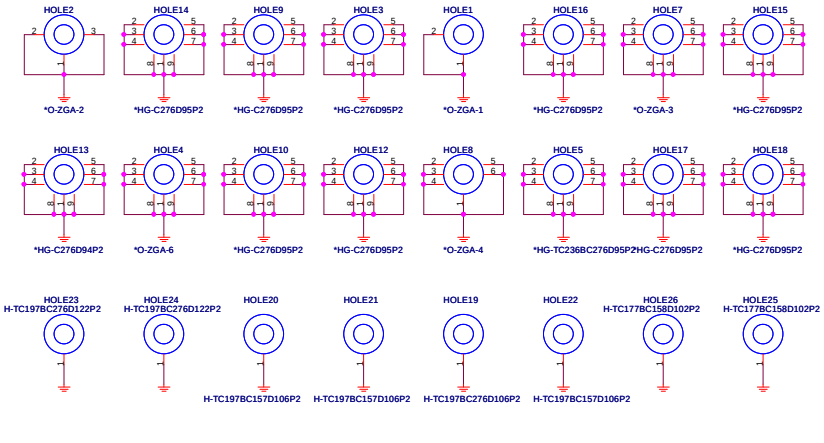
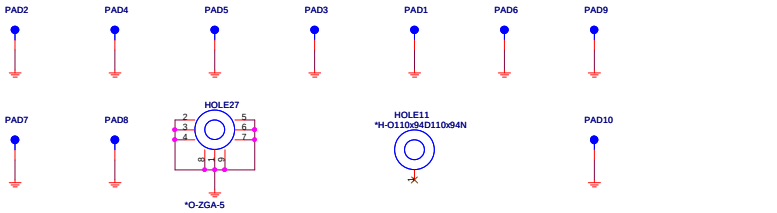

Codec(ADO)
HEADPHONE
Power (ADO)
Demodulation Filter L65 Place close to Codec
Mute(ADO)
Internal Speaker
System MIC
(Vista Premium Version)
Placement near Audio Codec
ANALOG
DIGITAL
Spilt by AGND
Spilt by PGND
Spilt by DGND
Normal Open Jack
Quanta Computer Inc.
PROJECT : ZGB
AUO/AMP
www.aitech1.ru

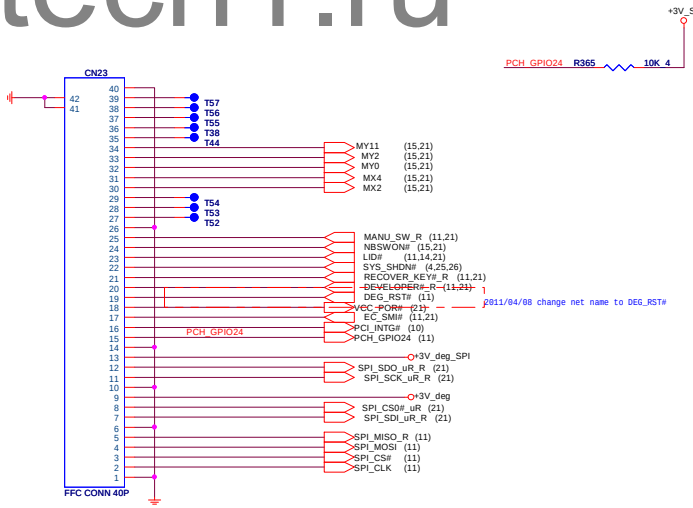












Quanta Computer Inc.		
PROJECT : Z6B		
Size	Document Number: USB on Board/LED/SW/HOLE/Debug port	Rev: 2A
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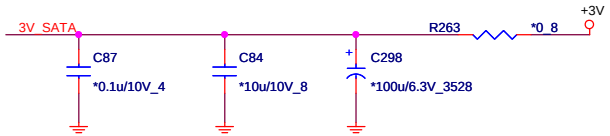

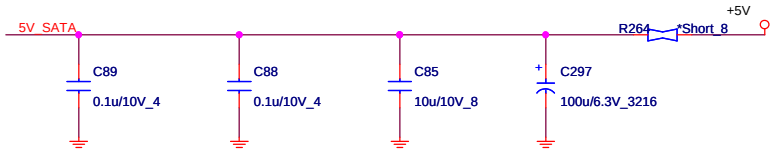

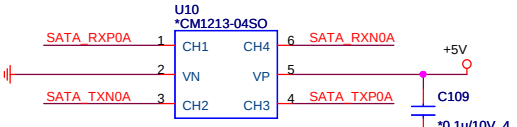

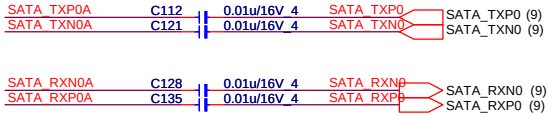

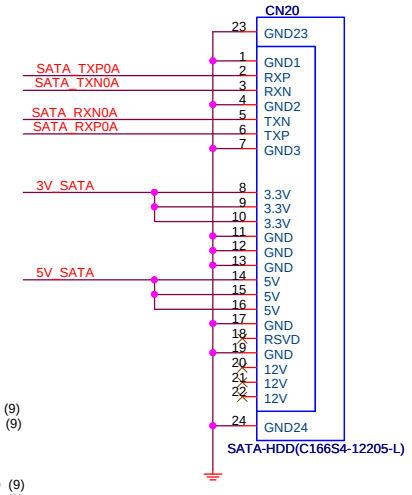

Quanta Computer Inc.

PROJECT : ZGB

Size	Document Number	Rev
	SATA-HDD/SSD	2A

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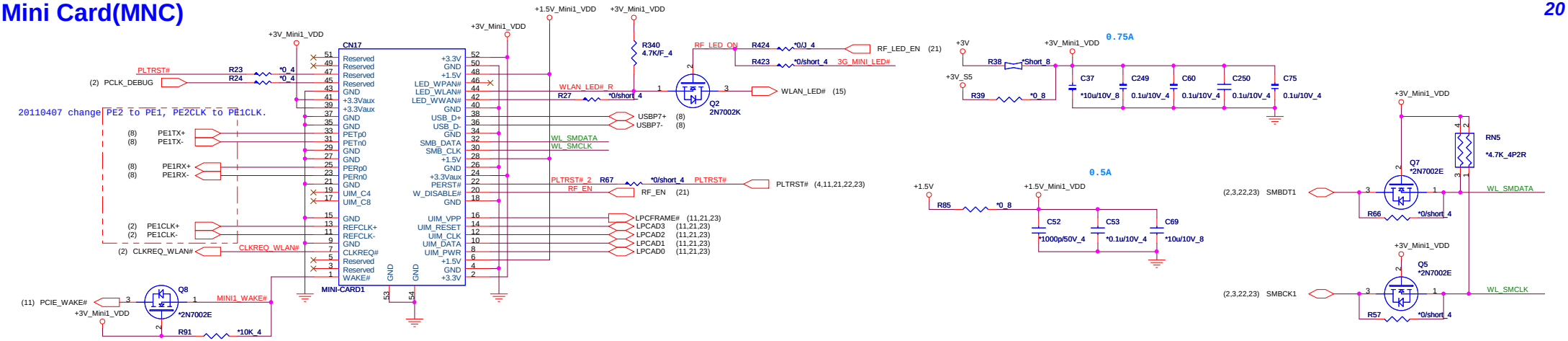
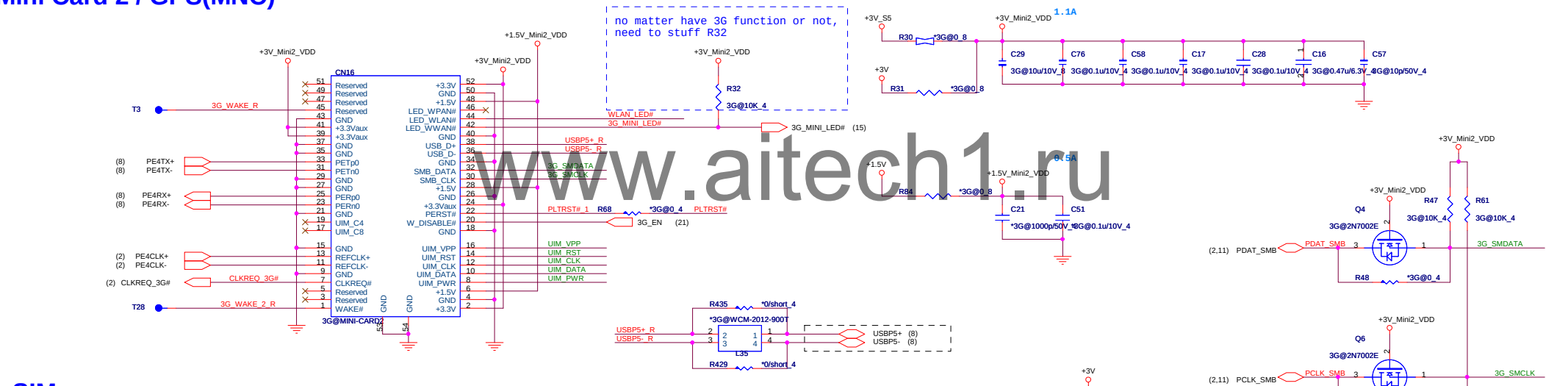
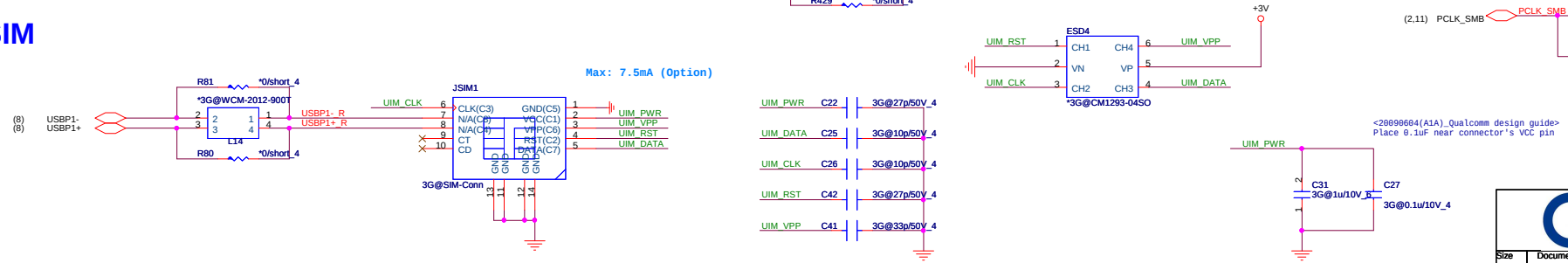
Mini Card(MNC)



Mini Card 2 / GPS(MNC)

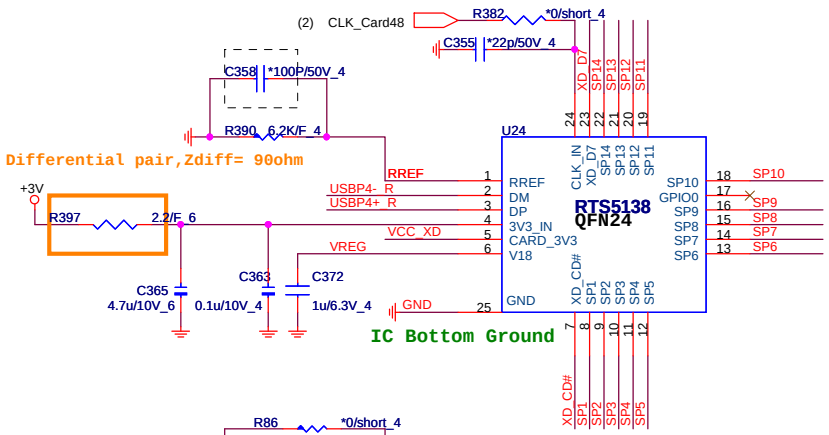


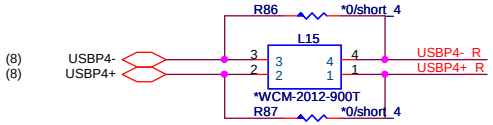
SIM

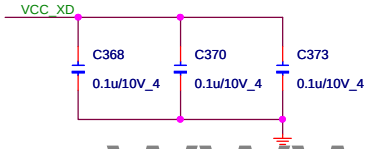


Quanta Computer Inc.		
PROJECT : ZGB		
Size	Document Number	Rev
	Mini-Card/WL/3G/SIM	2A
Date: Friday, April 08, 2011	Sheet 19 of 34	

RTS5138

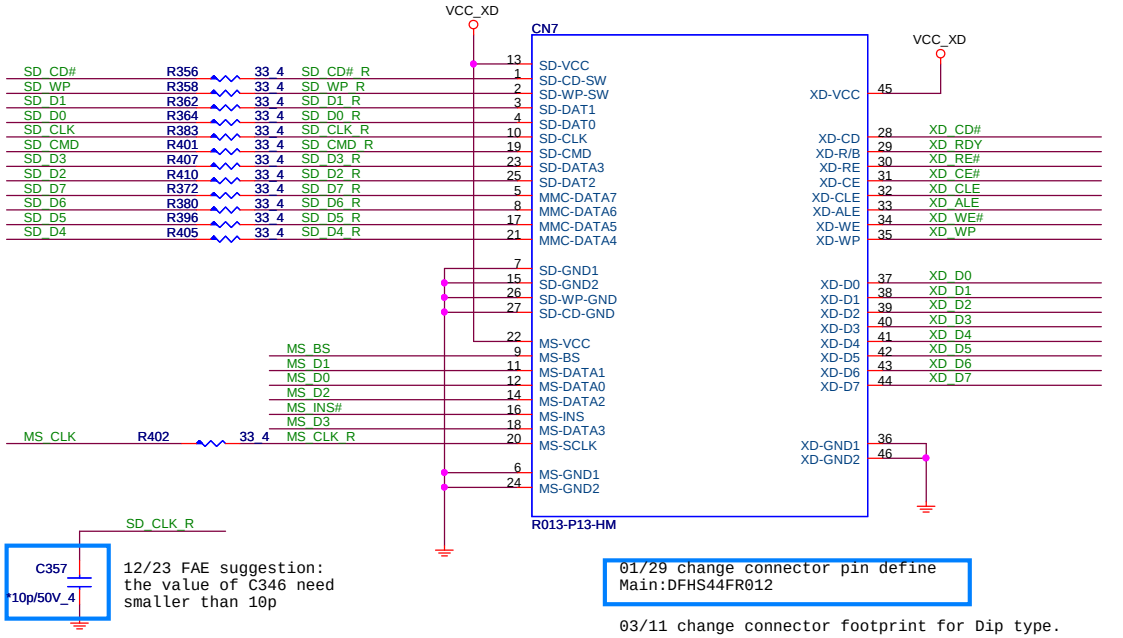






	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	
SP14	XD_D6		MS_BS
	XD_D7		

Share Pin



12/23 FAE suggestion:
the value of C346 need
smaller than 10p

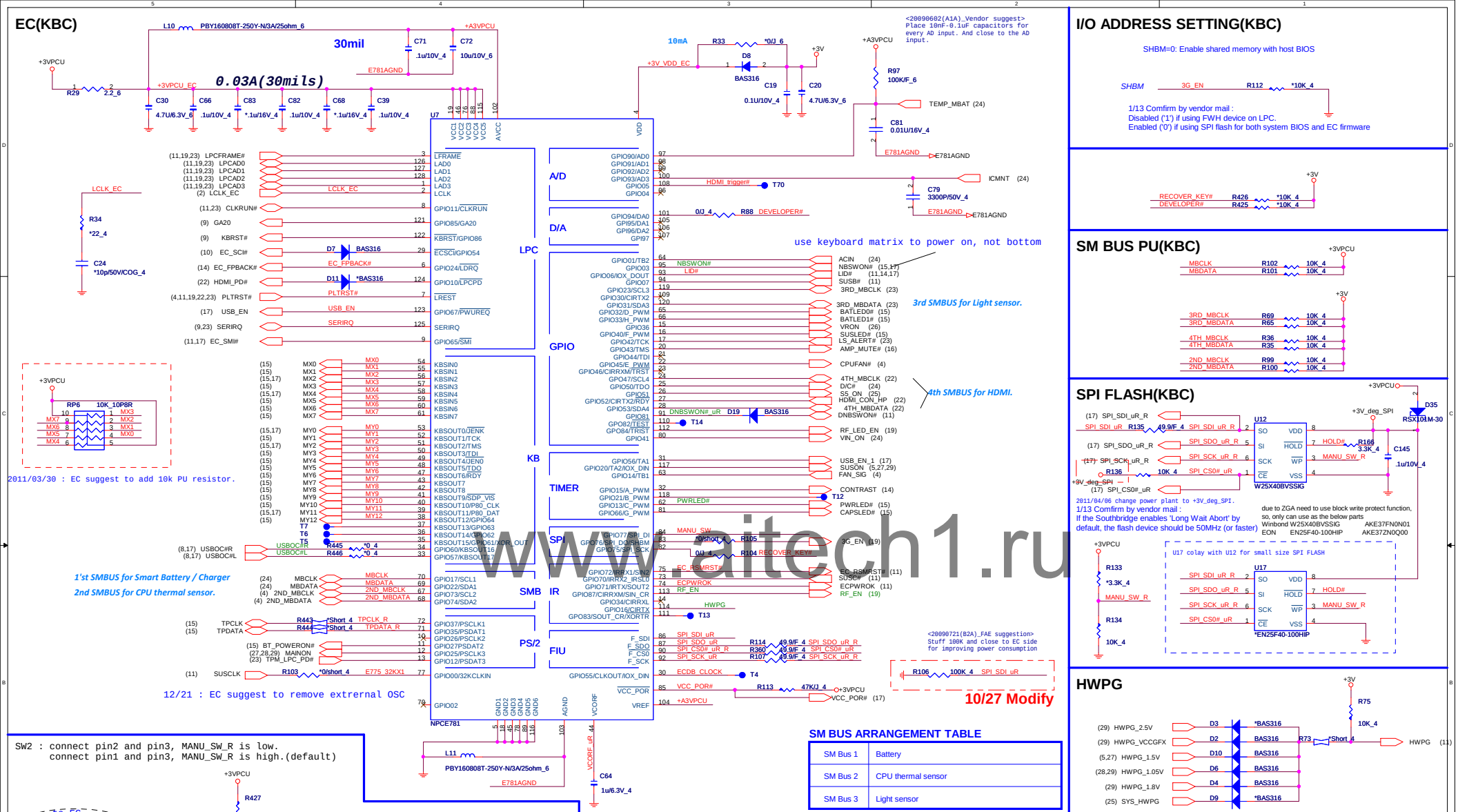
01/29 change connector pin define
Main:DFHS44FR012

03/11 change connector footprint for Dip type.

Quanta Computer Inc.
PROJECT : ZGB

Size	Document Number	Rev
	RTS5138	2A
Date: Friday, April 08, 2011	Sheet 20 of 34	

EC(KBC)



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	CPU thermal sensor
SM Bus 3	Light sensor

I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS

SHBM — 3G_EN — R112 *10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

RECOVER_KEY# — R426 *10K_4
DEVELOPER# — R425 *10K_4

SM BUS PU(KBC)

MBCLK — R102 10K_4
MBDATA — R101 10K_4

3RD_MBCLK — R69 10K_4
3RD_MBDATA — R65 10K_4

4TH_MBCLK — R36 10K_4
4TH_MBDATA — R35 10K_4

2ND_MBCLK — R99 10K_4
2ND_MBDATA — R100 10K_4

SPI FLASH(KBC)

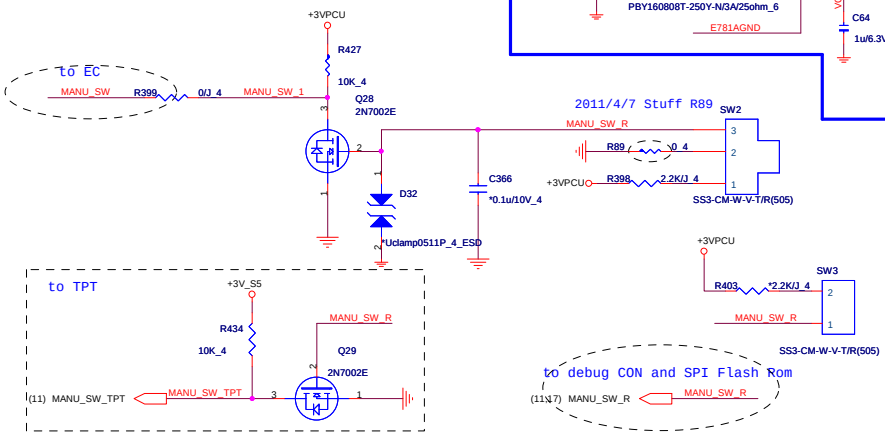
HWPG

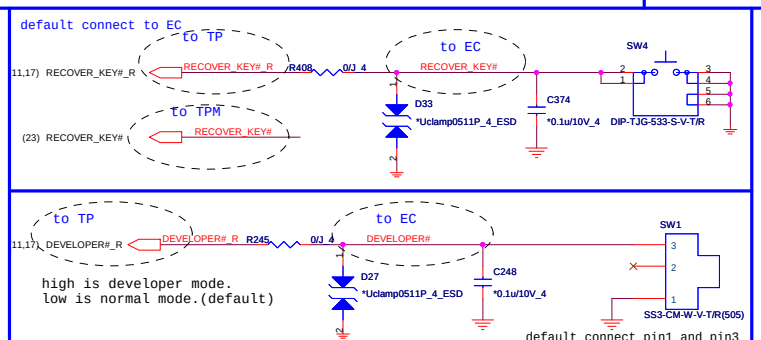
INTERNAL KEYBOARD STRIP SET(KBC)

10/26 UnStuff

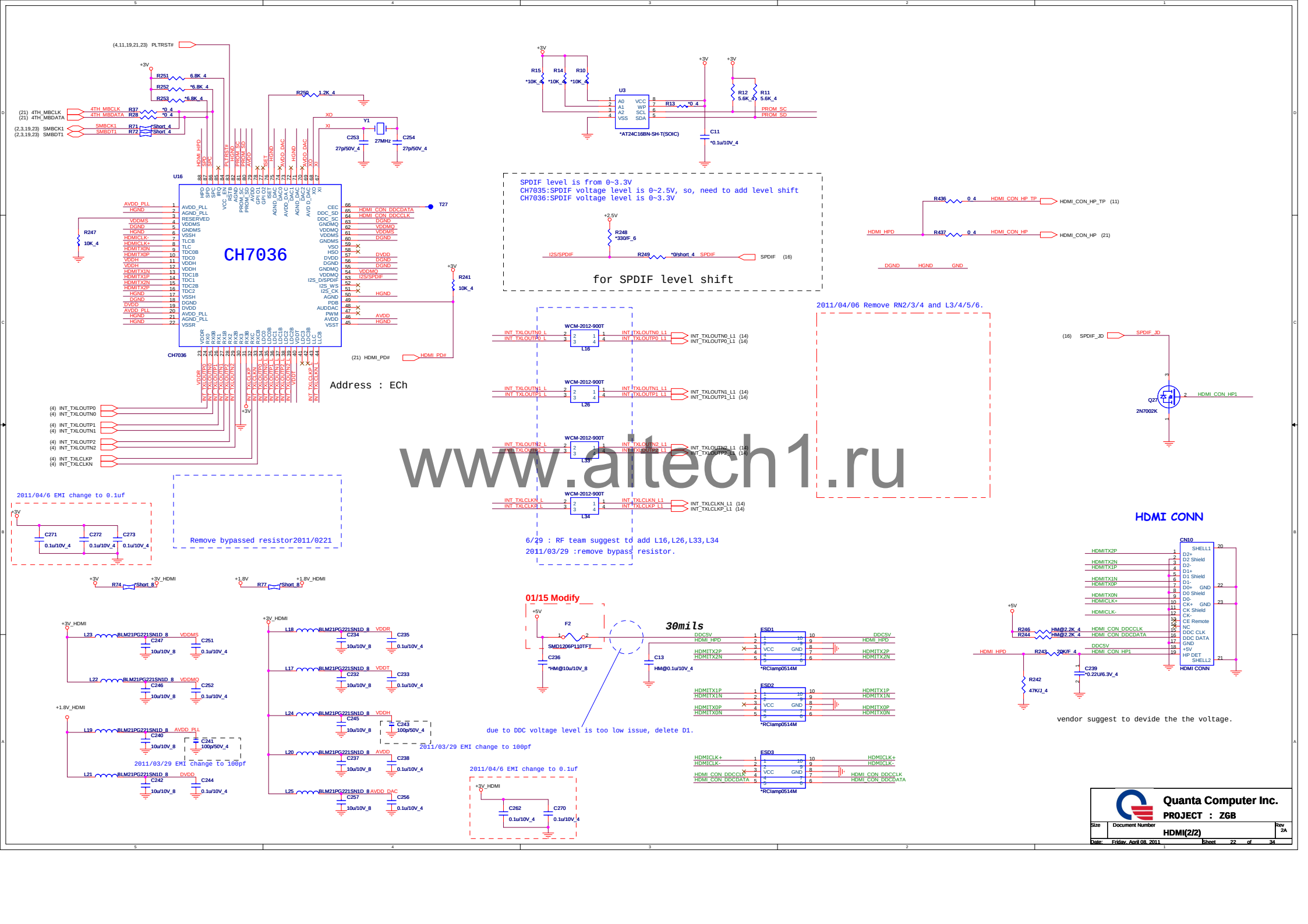
MY0 — R78 *10K_4 — +3VPCU

SW2 : connect pin2 and pin3, MANU_SW_R is low.
connect pin1 and pin3, MANU_SW_R is high.(default)





Quanta Computer Inc.				
PROJECT : ZGB				
Size	Document Number			Rev
	WPCE781 & FLASH			2A
Date: Friday, April 08, 2011		Sheet 21	of	34


CH7036
Address : ECh
SPDIF level is from 0~3.3V
CH7035:SPDIF voltage level is 0~2.5V, so, need to add level shift
CH7036:SPDIF voltage level is 0~3.3V
for SPDIF level shift
2011/04/06 Remove RN2/3/4 and L3/4/5/6.
Remove bypassed resistor2011/0221
2011/04/6 EMI change to 0.1uf
6/29 : RF team suggest to add L16,L26,L33,L34
2011/03/29 :remove bypass resistor.
01/15 Modify
30mils
due to DDC voltage level is too low issue, delete D1.
2011/03/29 EMI change to 100pf
2011/04/06 EMI change to 0.1uf
HDMI CONN
vendor suggest to devide the the voltage.
www.altech1.ru
Quanta Computer Inc.
PROJECT : ZGB
HDMI(2/2)
Rev 2A
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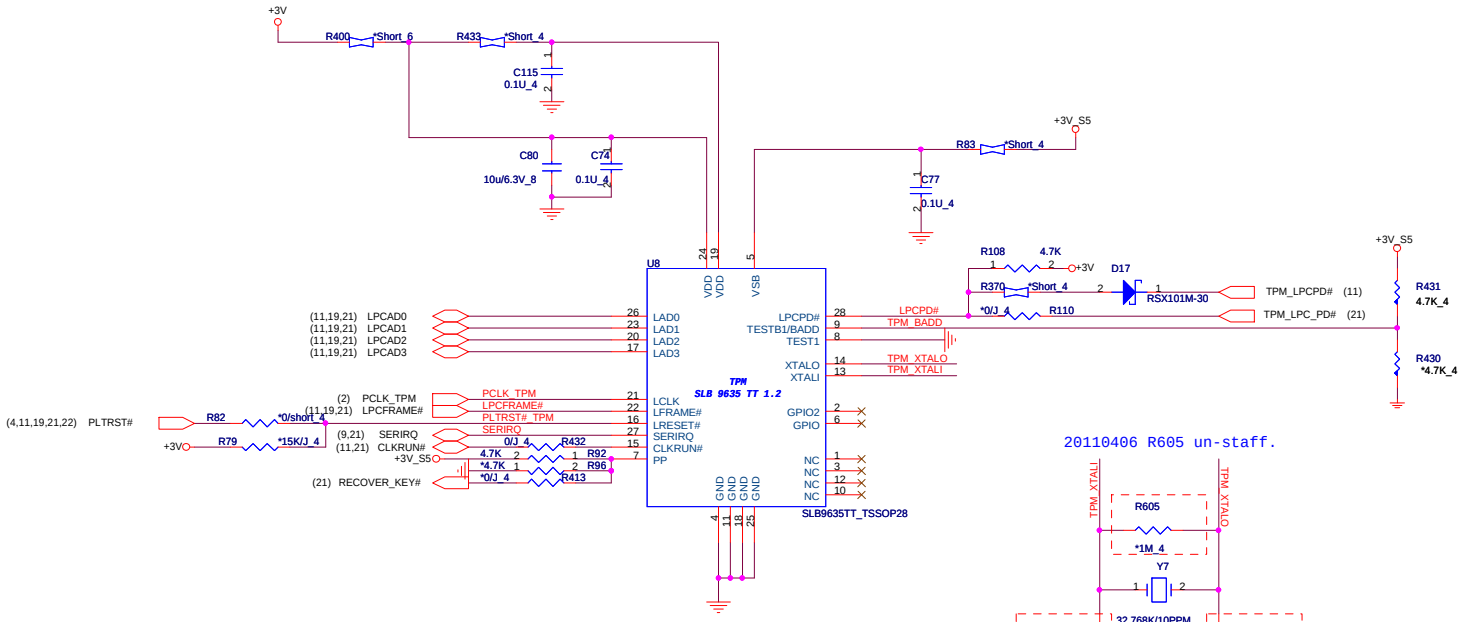
TPM

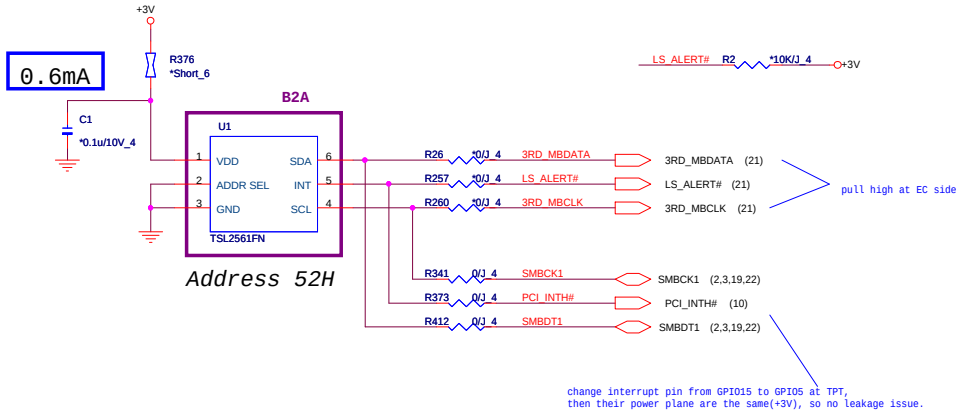


20110406 R605 un-staff.

	Resiger Base Address
BADD=0	2E / 2F
BADD=1 (default)	4E / 4F

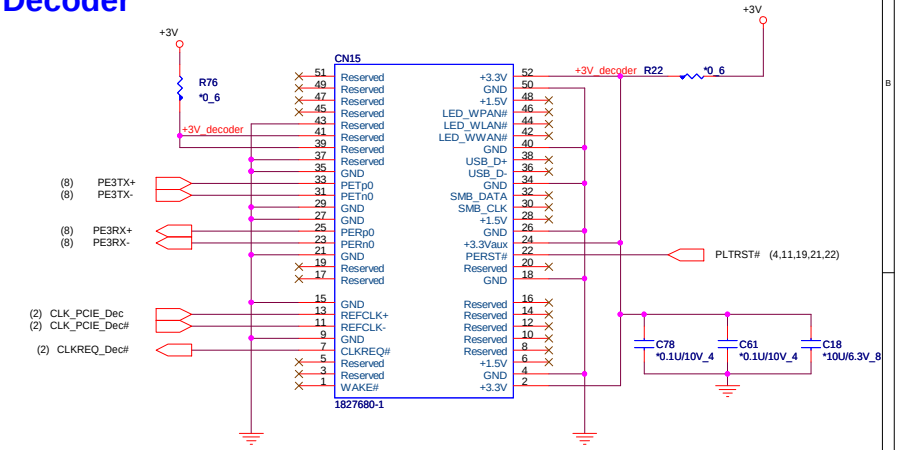
Light Sensor(LSR)

connector to EC, just stuff R2,R26,R257,R260
connector to TPT, just stuff R341,R373,R412



Video Decoder

dont need to stuff first, use innr document to add it.



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Size	Document Number		Rev
	Light/G-Sensor/GPS/TPM/Deco		2A
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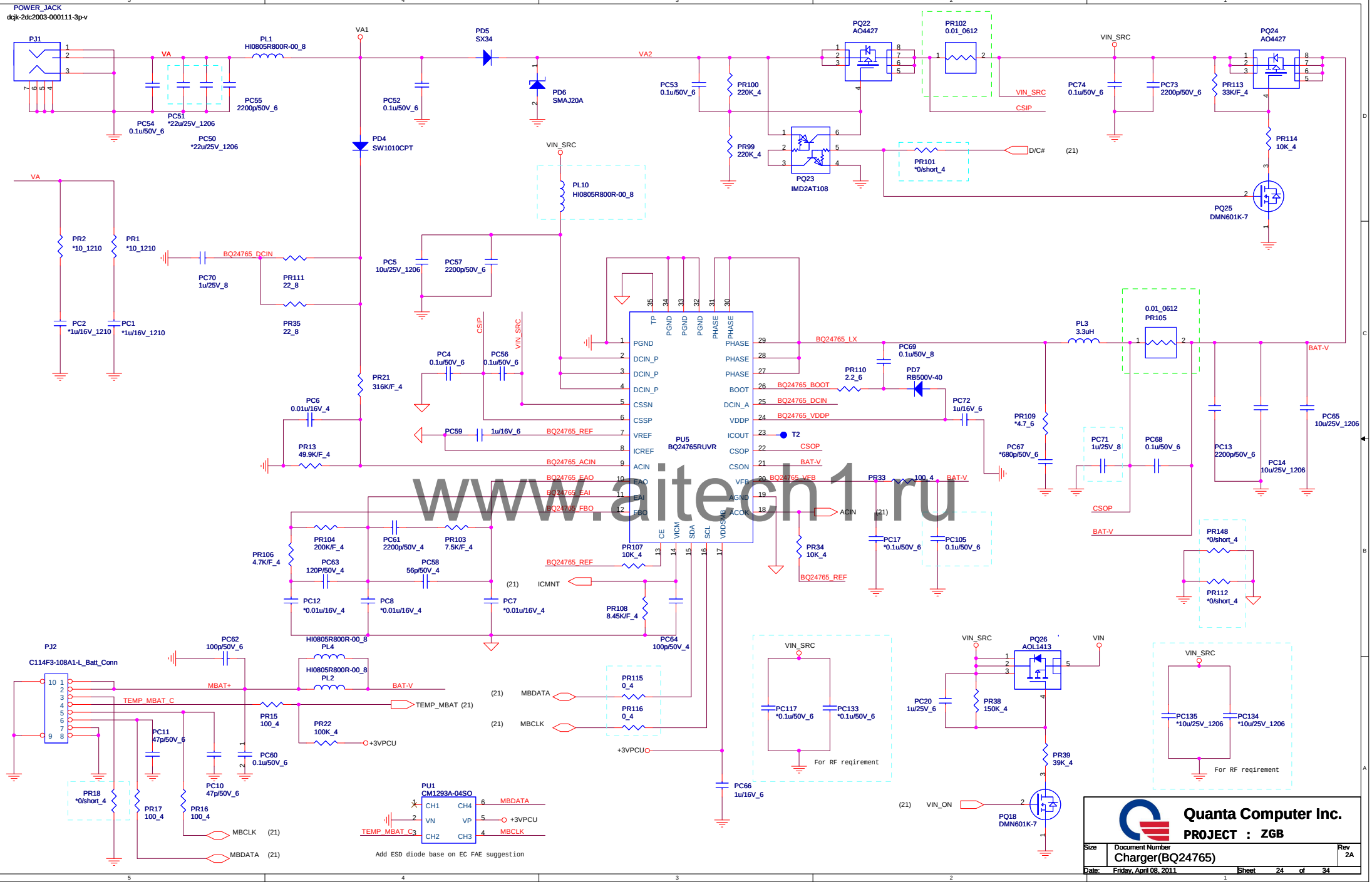
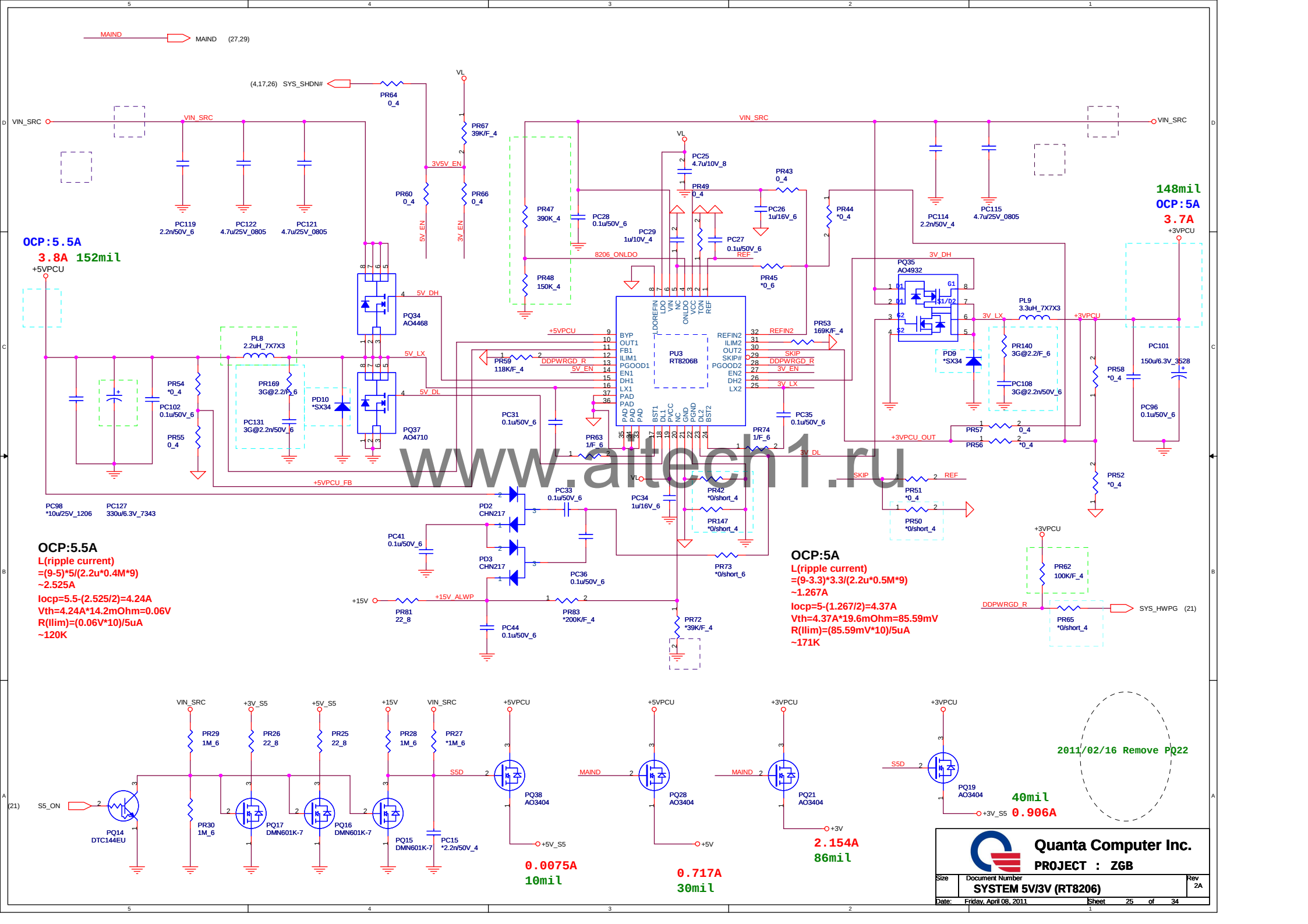
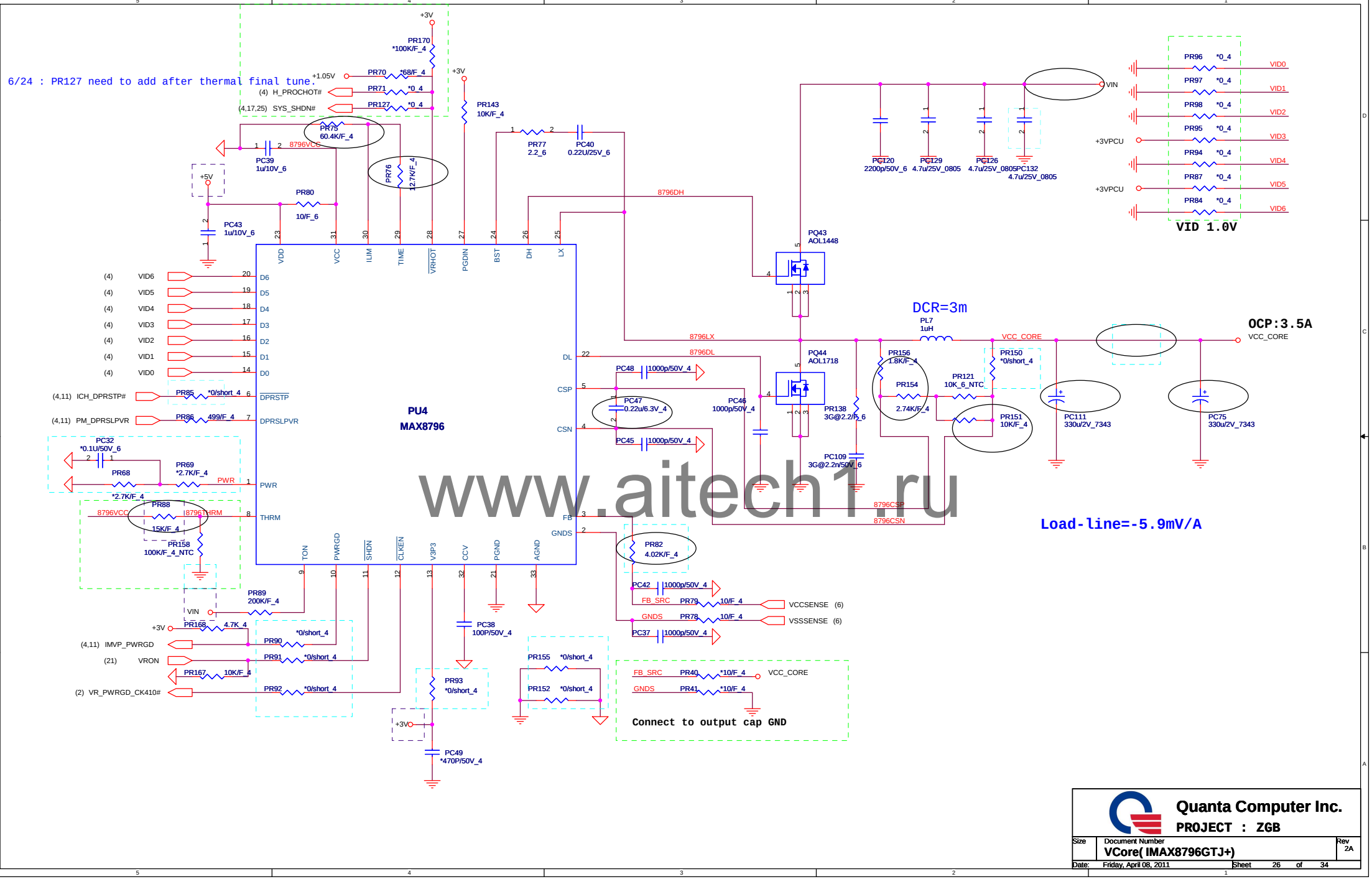
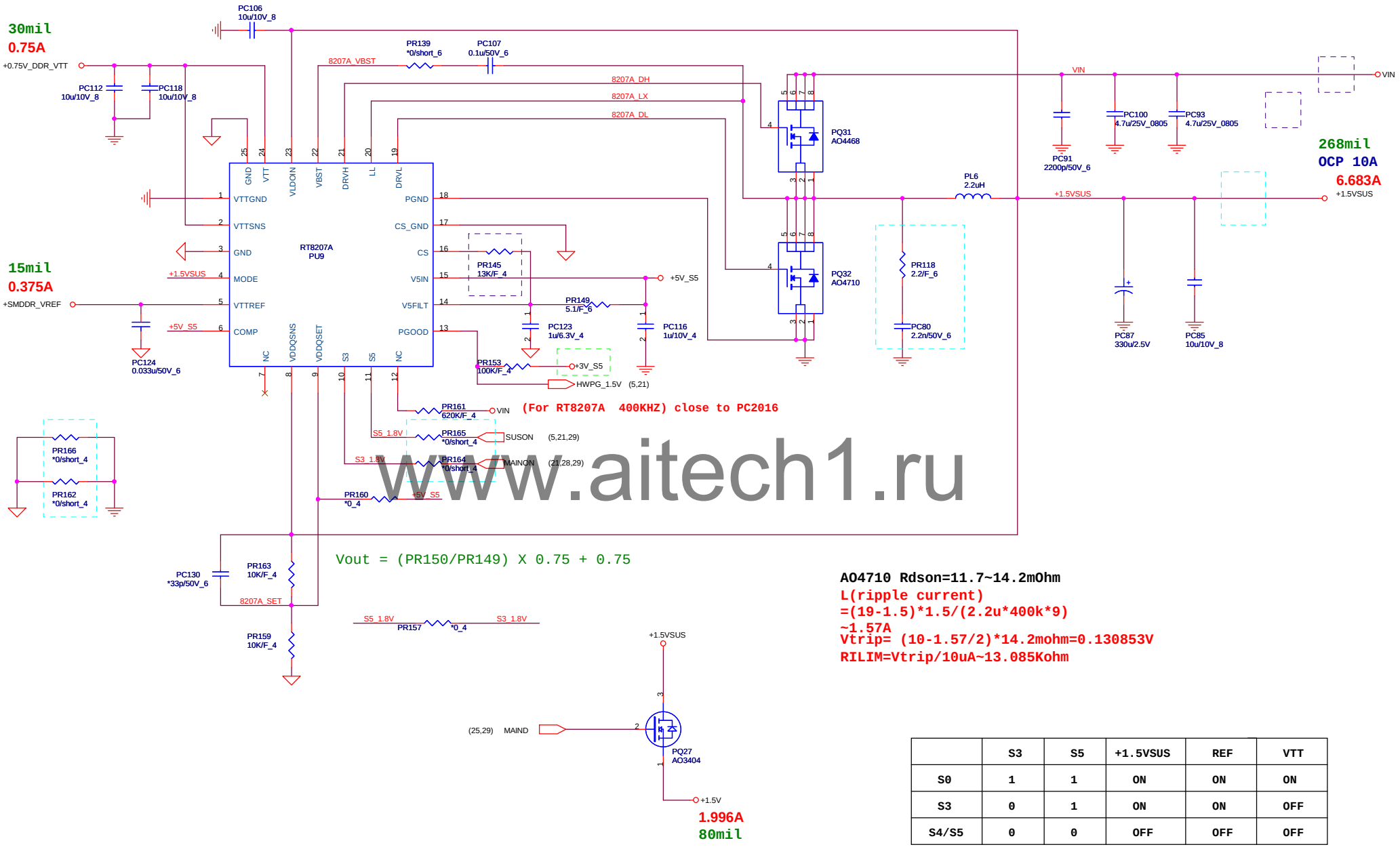






[PWM]



	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

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	DDR 1.5V(TPS51116)	2A

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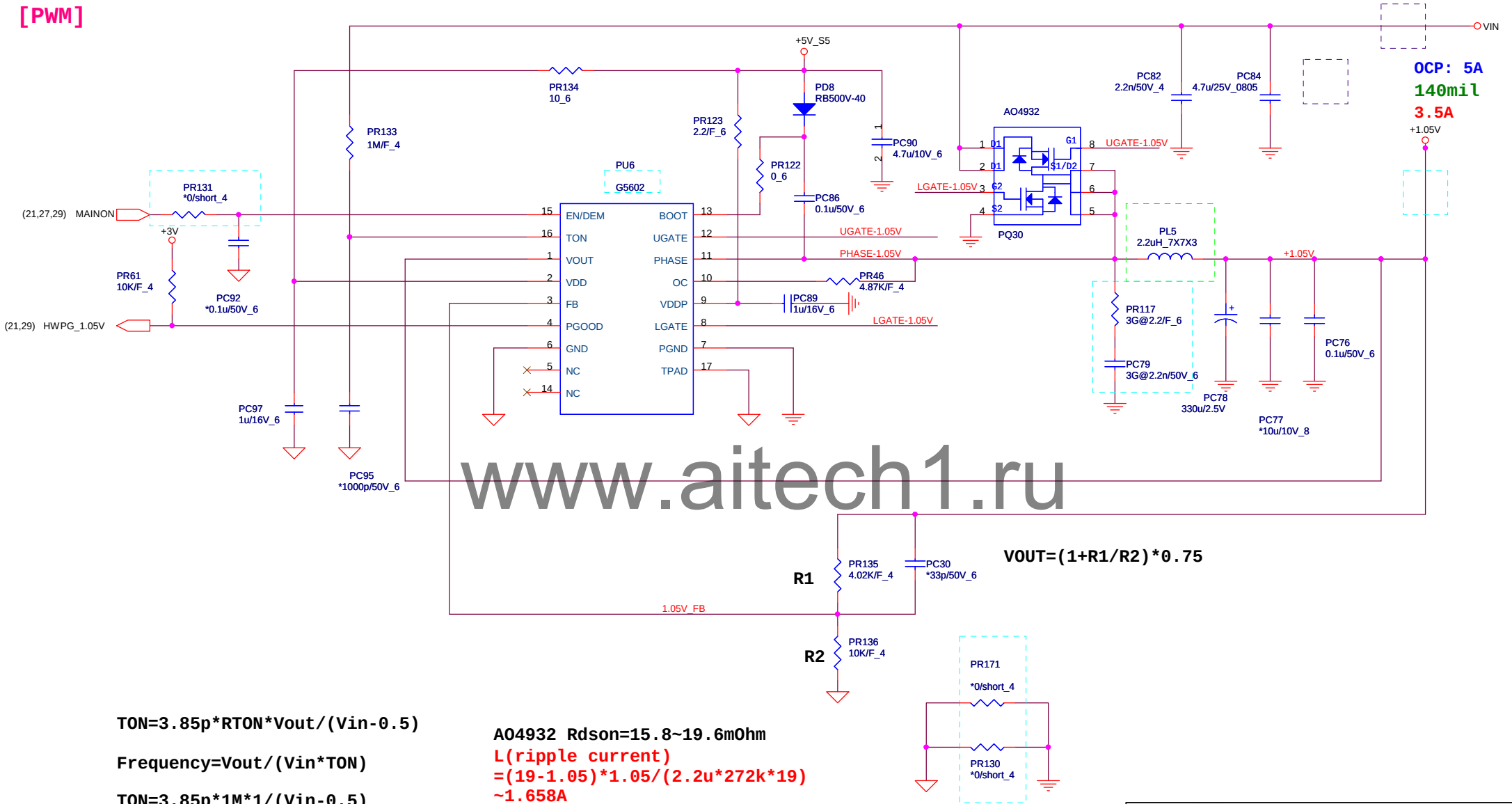
[PWM]



VOUT=(1+R1/R2)*0.75

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4932 Rdson=15.8~19.6mOhm

L(ripple current)
=(19-1.05)*1.05/(2.2u*272k*19)
~1.658A

Rth=19.6m*(5-0.829)/20uA

RILIM=4.087Kohm

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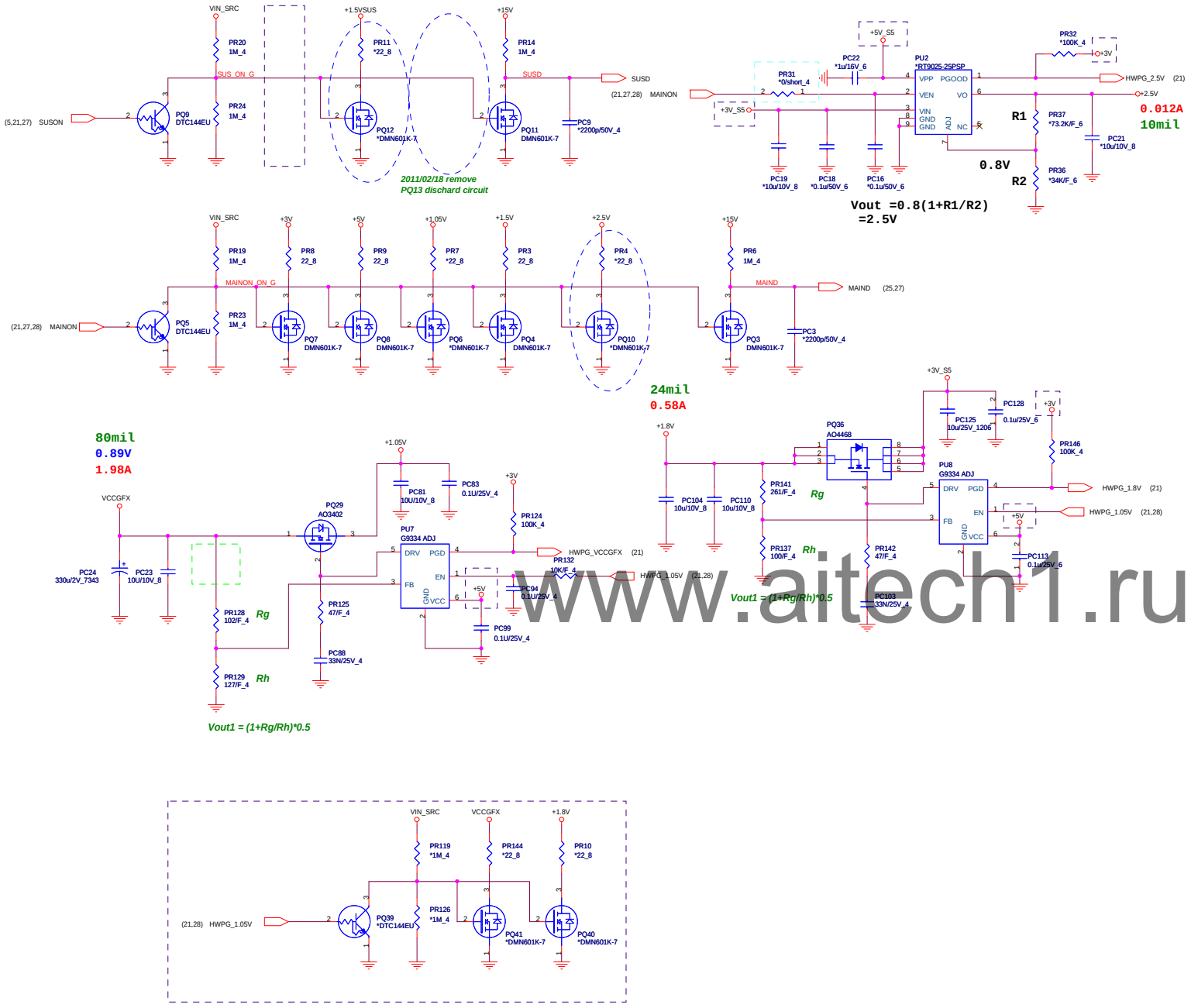

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	Discharge/1.8V)	2A

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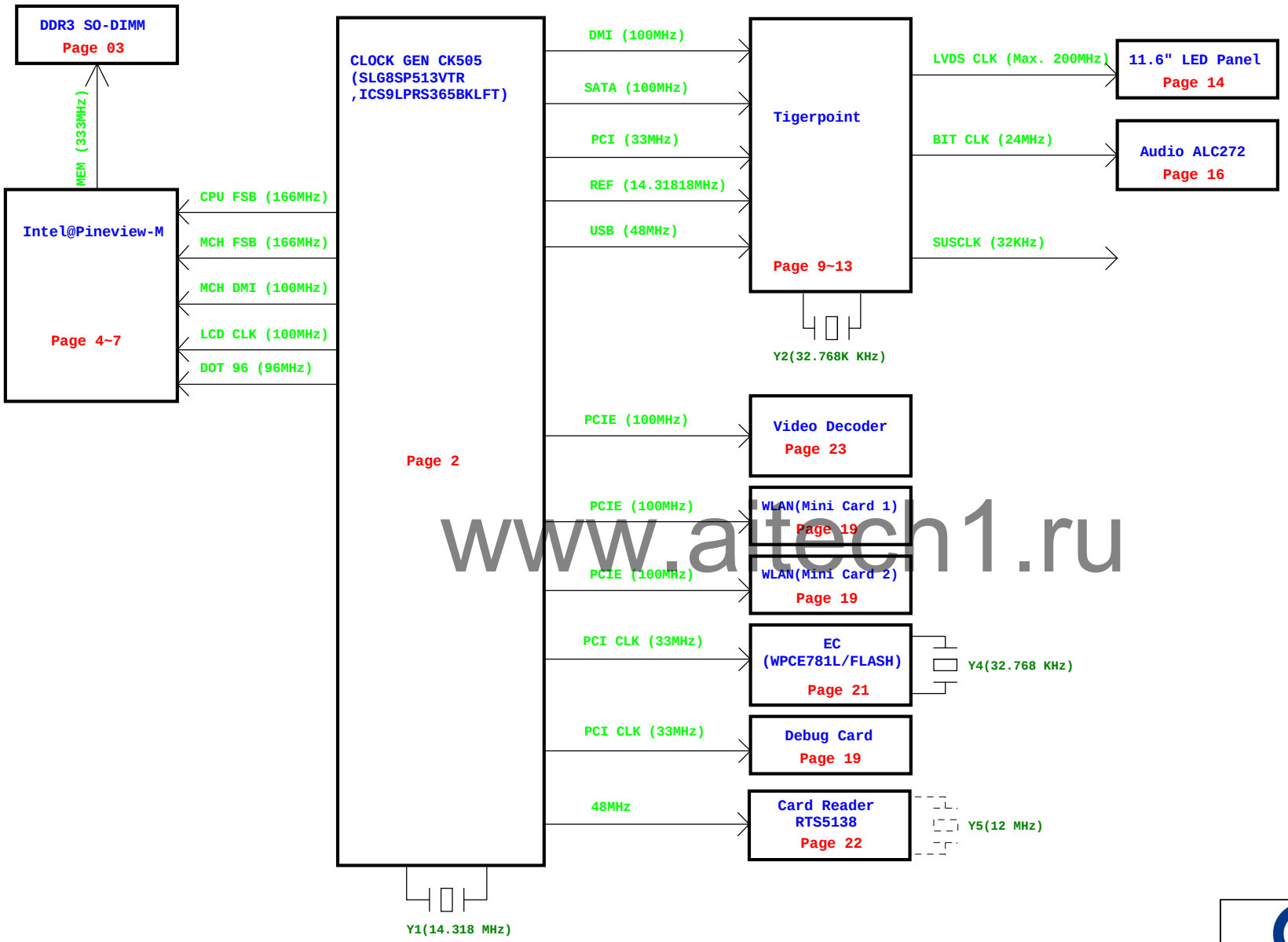

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	Clock Distribution Diagram	2A
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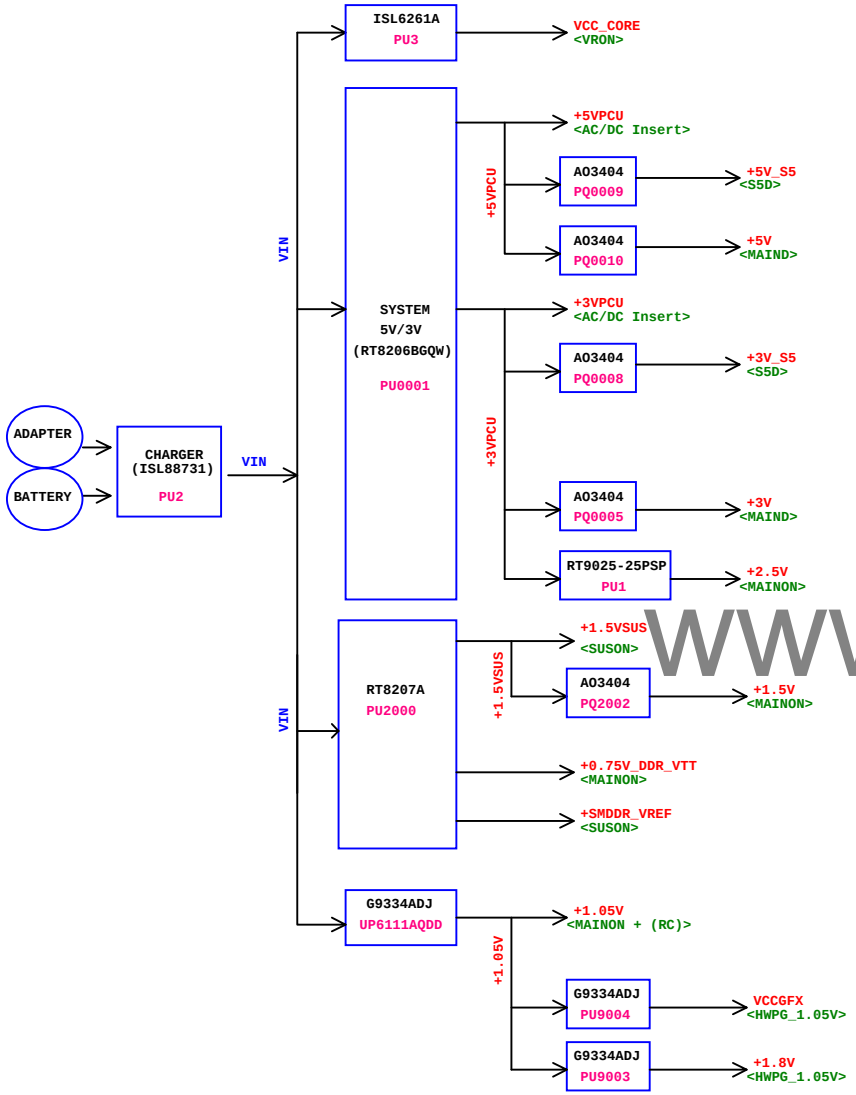

POWER	Distribution
VIN	LCD Backlight
VCC_CORE	CPU
+5VPCU	USB Connecter
+5V_S5	RTC, TPT
+5V	TPT , CRT , TouchPad , Codec , SATA , FAN , HDMI
+3VPCU	RTC, Hall Sensor, Light Sensor, EC, BIOS
+3V_S5	TPT , LAN , LAN EEPROM , RJ45 LED ,3G
+3V	CLK_GEN, CPU, TPT , LCD , CCD, DMIC, BT, Codec, WLAN/Wimax, Card reader, EC, DDR, HDMI
+1.5VSUS	DDR
+1.8V	CPU, HDMI
+1.5V	CPU, TPT
+0.75V_DDR_VTT	DDR
+SMDDR_VREF	CPU, DDR
+1.05V	CLK_GEN , CPU, TPT
VCCGFX	CPU
+2.5V	HDMI

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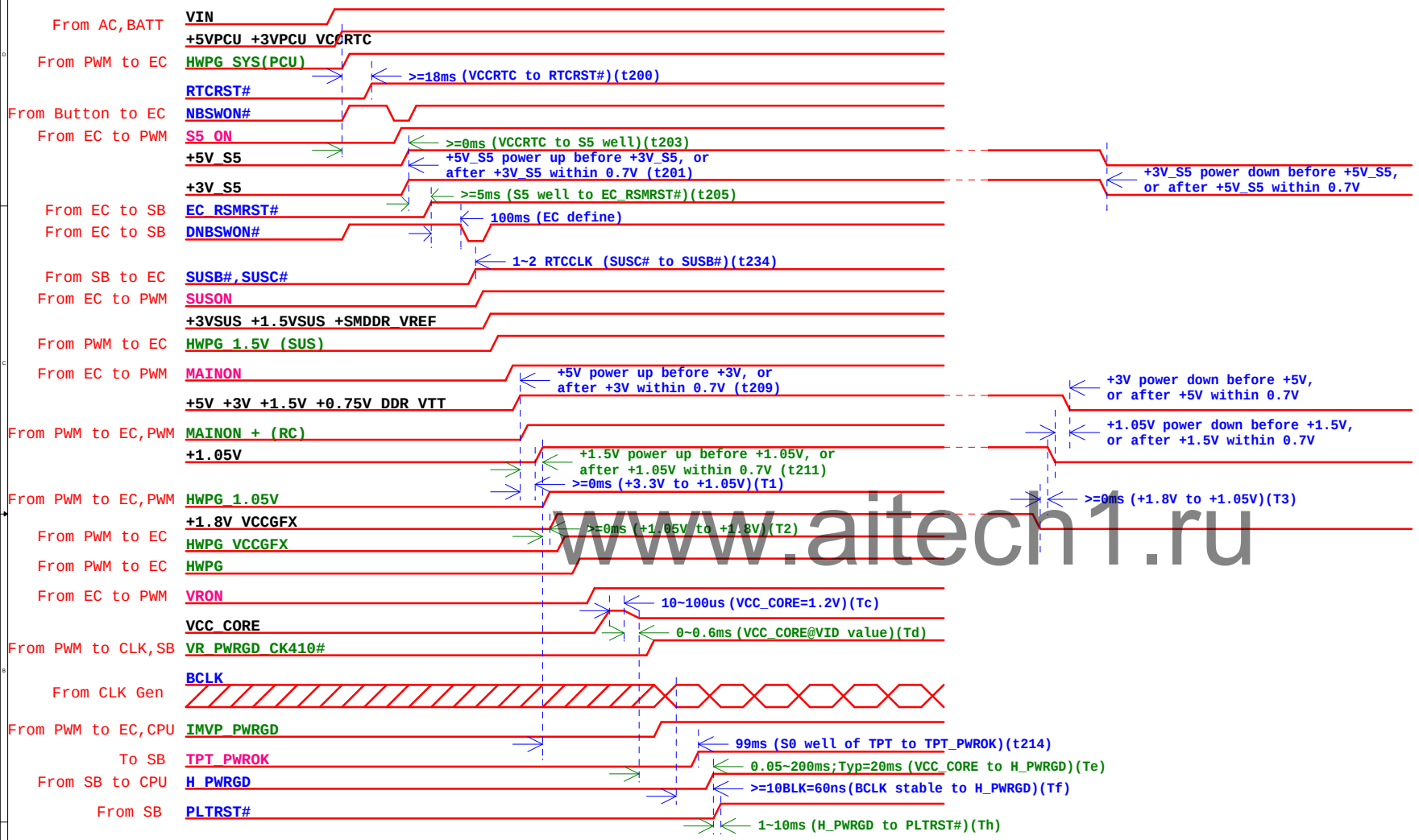
ZGA Power On Sequence



***Note: EC will sampling SUSB# & SUSC# every 5ms.**

ICH SMBUS Table

	CLK GEN	RAM	Mini Card (WLAN)	Mini Card (3G)
(SMB_DATA)/(SMB_CLK) (+3V_S5)	V	V	V	V
Power Plane	+3V	+3V	+3V	+3V_SUS
MOS CKT (Level shift)	Stuff	Stuff	*Reserve	Stuff

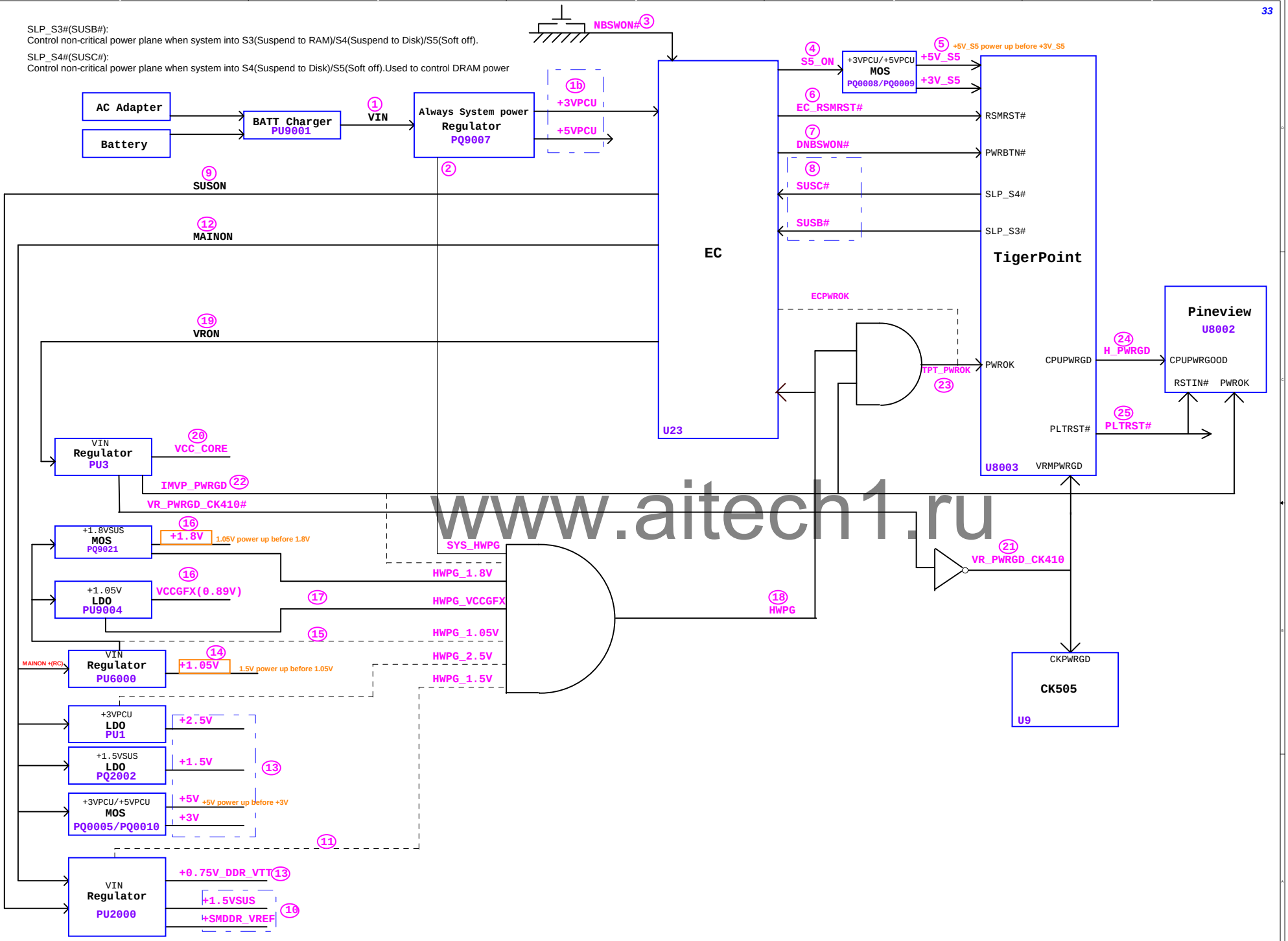
*Reserve: There is not SMBUS function in AVL

EC SMBUS Table

	Battery	CPU thermal Sensor	Light Sensor
EC781 SDA1 / SCL1 (+3VPCU)	V		
EC781 SDA2 / SCL2 (+3V)		V	
EC781 SDA3 / SCL3 (+3VPCU)			V
Power Plane	+3VPCU	+3V	+3VPCU
MOS CKT (Level shift)	X	X	X

SLP_S3#(SUSB#):
Control non-critical power plane when system into S3(Suspend to RAM)/S4(Suspend to Disk)/S5(Soft off).

SLP_S4#(SUSC#):
Control non-critical power plane when system into S4(Suspend to Disk)/S5(Soft off).Used to control DRAM power



Quanta Computer Inc.
PROJECT : Z6B
power sequence block diagram
Rev 2A
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Model	REV	CHANGE LIST	MODEL	ZGB FROM X	ZGB To 2A
ZGB MB	A1 (V1.0)	page 29 :Change PQ33 to PQ43,PQ44 for CPU change to dual core.			
		page 29 : change PC75 from 220uf to 330uf. becasue dual core CPU need adjustment.			
		page 29 : change PC111 from 330uf to 220uf becasue dual core CPU need adjustment.			
		page 29 : change PR151 from 1.8K to 10K becasue dual core CPU need adjustment.			
		page 29 : change PR156 from 1.6K to 1.8K becasue dual core CPU need adjustment.			
		page 29 : change PR154 from 1.1K to 2.7K becasue dual core CPU need adjustment.			
		page 29 : change PC47 from 0.1uf to 0.22uf becasue dual core CPU need adjustment.			
		page 29 : change PR82 from 1.2k to 4.02k becasue dual core CPU need adjustment.			
		page 29 : change PR88 from 15k to 13k becasue dual core CPU need adjustment.			
		page 29 : change PR76 from 18k to 12.7k becasue dual core CPU need adjustment.			
		page 29 : change PR57 from 53.6k to 60.4k becasue dual core CPU need adjustment.			
		page 2: change CLK GEN from SLG8SP513VTR to SLG8LV631VTR for power saving.			
		page 11: change RTC from connector to socket for SMT request.			
		page 23: TPM change to Infineon replacement R428,R38,R433,C77,R83,R82,R96,R431,C756,C765,Y7,R432			
		page 29 : change net name VCC_CORE to VCC_CORE_1 for net name adjustment.			
		page 17 : Add debug port 40pin for customer reqeust.(2011/02/27)			
		page 09 : Delete 10pin debug port and add test point on PCH debug pin.(2011/01/31)			
	A1 (V1.1)	page 15: Base on customer request Reserve BT circuit.(2011/02/01)			
		page 17: CN23 add test point Pin7,8,11,12,13,21,27,28,29,35,36,37,38,39 for NC pin.(2011/02/01)			
		page 21: Add 0ohm on SMB clk and SMB Data for test use.(2011/02/01)			
		page 15: Add PCH SMB CLK and data to TP SMB clk and data and additional MOS to prevent electric leakage for reserve test use.(2011/02/01)			
		page 14: Add +5V CCD power for OV9726 CCD and reserve +3V CCD power.(2011/02/01)			
	A1 (V1.2)	page 14: Change to +3V CCD power and reserve +5V CCD power.(2011/02/01)			
		page 23: 1.remove break net U8.10 to U8.24. 2.R96->NI, change R92 to pull to +3V_S5 (leave NI)3.populate Y7/C756/C765/R605. R605->1M, C756/C765->12pF4.populate R428, populate R431. Change R431 pull to +3V_S5.5.add populated 0R jumper U8.28 to U20.G22, change R108 pullup to +3V_S5			
		page 17: R359-361, R363, R366 are not required remove CN23 Pin7,8,11,12,13 conector to KBC EC ROM. CN23 Pin22 connector to SYS_SHDN#(2011/02/10)			
		page 14: add resistor between Rom and Tigerpoint of U20 pin M8(2011/02/10)			
		page 21: add resistor between SPI Rom and KBC of U7pin 90,Remove 0ohm on U7 pin71,72. because separate I2C circuit.2011/02/10)			
		page 15: Add a connector and circuit for TPD I2C circuit, but SPEC acer not yet confirm.(2011/02/10)			
	A1 (V1.3)	page 15: Follow up synatic pin define modify TPD I2C circuit.(2011/02/11) Pin 6 => CLK/Pin 5 => GND/Pin 4 => DAT/Pin 3 => VDD/Pin 2 => NC/Pin 1 => INT(interrupt)			
		page 17: Change CN23 Pin15 PCH_GPIO24_D net name to PCH_GPIO24(2011/02/11).			
		page 23: Add one 0R ahead U1 pin1,R76 and R22 change from 0402 to 0603,for power consumption measure.(2011/02/11).			
	A1 (V1.4)	page 23: LPCPD R108 change +3V_S5 to +3V well.Add diode between U20.G22 and U8.28 to ensure well isolation.(2011/02/14).			
		page 15: 1.Remove R439,L37 becasue not use +5VSUS option.2.Change CN3 from 4pin to 6pin 3.Add CN8 for PS2 TPD option.(2011/02/15)			
		page 02: C768, C774 and C772 change from 10U/10V_8 to 10U/6.3V_6. .(2011/02/15)			
		page 17: C268, C266 and C297 change from 100u/6.3V_3528 to 100u/6.3V_3216 .(2011/02/15)			
		page 11: D34 change to 30V 1A diode .(2011/02/15)			
		page 17: D35 change to 30V 1A diode and Delet D36 only use one diode.D4/6/10 remove NI.(2011/02/15) .			
		page 15: Follow up pin define modify TPD I2C circuit.(2011/02/15) Pin 6 => VDD/Pin 5 => SCL/Pin 4 => SDA/Pin 3 => HINT/Pin 2 => SINT/Pin 1 => GND			
	A1 (V1.5)	page 25: Remove PQ42 becasue not +5VSUS supply(2011/02/16)			
		page 12: change R209 and R194 from 0603 to 0805 for current limitation .(2011/02/16)			
		page 11: Change U20 A24 net name from MBID2 to SNIT_TP U20 D19 net name change PCH_GPI026 to HINT_TP, for TP I2C interrup, CN3 pin3 change net to HINT_TP and pull up +3V_S5,PCH_GPI039 leave test point.			
		page 08: R294 and R285 to remove NI for PCH control.			
		page 21: R112 leave NI,R97 pull up change to +A3PCU power wall,remove U7 pin96 net name because dulipcate, add NI 0 ohm on U7 PIN34/33 for EC option.			
	A1 (V1.6)	page 11: R277,R276 from 8.2k change to 10k ,R195/R188 10k to 8.2k pull up following intel spec.			
		page 17: Update CN23 P/N and footprint for pitch0.5.			
		page 21: R102/R101/R69/R65/R36/R35/R99/R100 change to 4.7k 0402 for supplier NVO suggestion.			
		page 23: D17 change diode to 30V 1A.			
		page 15: Swap CN3 pin define Pin 1 => VDD/Pin 2 => SCL/Pin 3 => SDA/Pin 4 => HINT/Pin 5 => SINT/Pin 6 => GND			
	A1 (V1.7)	page 23: U8. PP pull down to GND.(2011/02/18)			
		page 11: Change TPD power well to +3V_S5.(2011/02/18)			
		page 25: Remove PQ22 +3VSUS power well.(2011/02/18)			
		page 29: Remove PQ13 and PR12 discharge circuit.(2011/02/18)			
		page 21: R102/R101/R69/R65/R36/R35/R99/R100 change to 10k 0402 for supplier NVO suggestion.			
		Change All +3VSU to +3V_S5 power plant.			
	B1 (V2.0)	page 22: Remove LVDS bypass resistor.(cancel LVDS stub trace)			
		page 16: Change C163 from 10u to 2.2uf.(follow Codec FAE suggestion.)			
		page 03: Add EMI CAP C258,C261,C260,C259 100pf.(EMI request.)			
		page 11/15: Remove I2C cricirt SNIT/HNIT and Change RTC charge limitation resistor to prevent charge current to large,R415 and R422. unstaff U14 and add R207 0ohm.(Follow Google commend to use 6pin P/S2 touch pad.)			
		page 15: Remove CN8 TP 4pin.(Following Google suggestion use 6pin connector.) CN6 from DFHD05MRD98 to DFWF05MR042 and BT power plant from +3VPUC to +3V_S5.(Follow acer AVAP to use new BT , so we have to use new connector, Correct wrong BT power supply.)			
		page 16: R16/R17 add 0ohm for EMI.(EMI request)			
		page 26: Remove vcore jump,(throse R for power consumption measurement, we won't use they after A stage.)			
		R615,R176,R148,R351,R280,R279,R281,R298,R207,R202,L30,R194,R329,R141,R256,R46,R56,R44,R254,R255, R125,R124,R131,R17,R16,R258,R324,.R98,R256,R210,R337,R287,R196,R292,R293,R198,R199,R217,R216,r26 4,R382,R73,R443,R444,R74,R78,R400,R433,R83,R370,R376, (Change 0ohm to short pad.(throse R for power)consumption measurement, we won't use they after A stage.)			
	B1 (V2.1)	page 15: add R261 and C410 for BT soft star.			
		page 11: change R152/210 power plant from +3V to +3V_deg.(for google suggestion.)			
		page 21: Add RP6 PU 10K ,(for keyboard lose key issue.)			
		page 21: R136 change power plant from +3VPCU to +3V_deg_SPI.(for google suggestion.)			
		page 22: Add C271/272/273/262/270 0.1uf(for EMI suggestion)			
		page 22: Remove RN2/3/4/5 and L3/4/5/6.(avoide HDMI stub trace.)			
		page 23: R605 un-staff.(for supplier suggestion becasue internal Rd 1Mohm.)			
	B1 (V2.2)	page 08: PE2RX+/- and PE2TX+/- swap to PE1RX+/- and PE1TX+/-.(WLAN change from PCIE2 to PCIE1. So BIOS can turn off PCIE2 alone and save power consumption)			
		page 19: PE2CLK+/- net name change to PE1CLK+/-.(PE2 already swap to PE1 so change net name.)			
		page 11: C96 change power plant to +3V_deg.(for google suggestion.)			
		page 11: Change R283 from short-pad to 0ohm and unstuff.Stuff U19 (AND gate) to increase fan-out (There are many devices use PLTRST#. TPT may not drive them so use AND gate to fan out)			
		page 21: Add R89 0ohm on SW2.2.(for google suggestion,reserve 0ohm.)			
	B1 (V2.3)	page 8: Change USBOC#R1 from OC6# to OC#0 base on usb port.(Wrong assign for USB OC change to correct)			
		page 11: Change U19 Pin1 to Deg_RST# pull 4.7K to +3V.(for google suggestion control PLTRST#)			
		page 17: Change CN23 Pin19 net name from PLTRST# to DEG_RST#.			

DOC NO.	PROJECT MODEL :	11.6	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISON:	

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Change list
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